

Emerging Technologies for VLSI Applications

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MITRE MIP Funding



Problem



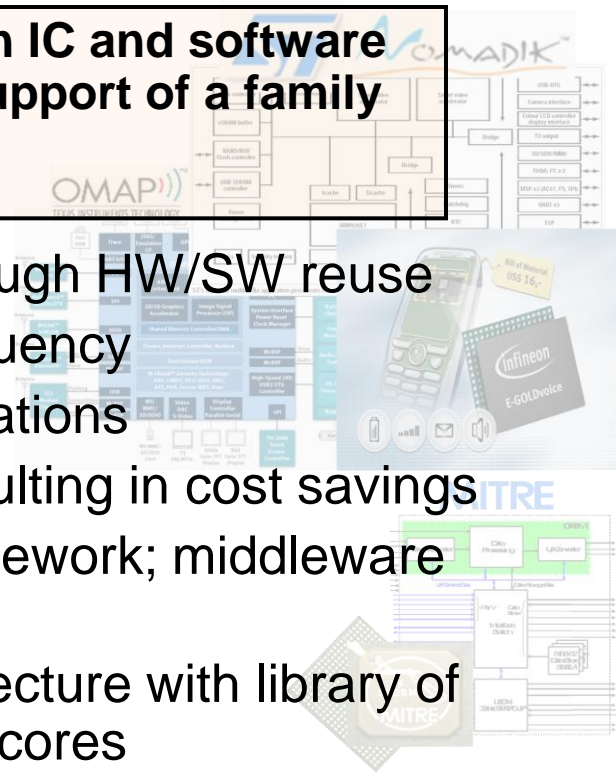
- **The Warfighter requires small, low-power, and more capable electronic equipment to identify and counteract threats**
- **The increased complexity in electronics systems is creating a USG dependence on COTS (e.g. FPGA), leading to increased SWaP to maintain system specifications and performance**
- **Today's microelectronics requires consideration of both hardware and software architectures as well as process technology and design flows to realize a practical solution for reducing SWaP**

Platform System-on-a-Chip (SoC)

Addressing the SWaP and Capability Challenge

Flexible capability consisting of an IC and software that is designed to be reused in support of a family of applications.

- Increased design efficiency through HW/SW reuse
- More MIPS/MOPS at lower frequency
- Lower power for portable applications
- Decreased time-to-field and resulting in cost savings
- Common SW development framework; middleware abstraction
- Common extendable HW architecture with library of functions: Leverage 3rd party IP cores



Objective



- **Maintain MITRE's lead advisory role in microelectronics by extending our capabilities into low power Platform SoC design to support the mission requirements of our sponsors**
- **Deliver a highly capable Platform SoC intellectual property (IP) core and prototype devices to demonstrate to the USG innovative solutions using state-of-the-art technology**
 - **Research low power architectures and semiconductor fabrication technology**
 - **Select impactful sponsor application**
 - **Develop and fabricate prototype Platform SoC**
 - **Deliver licensable intellectual property (IP) core**

Activities



- **Studies (Multicore, SDR, and JTRS)**
- **Selected tactical radio as application target**
 - **SDR-on-a-Chip (SDRoC)**
 - **High volume military application**
 - **Support for legacy and next gen networking waveform**
 - **SINGARS and SRW**
- **Waveform sizing and benchmarking**
 - **Currently benchmarking SINGARS on ARM-based emulation system**
 - **Working collaborative industry relationships for SRW**
- **Preliminary architecture and design**
 - **Multiple ARM Microprocessors**

MITRE's First 90 nm Low Power SoC

- Low power transceiver device – Completed FY07
- IBM 9LP 90nm Low-Power CMOS
- 9-layer metal stack (Cu)
- Die size: 5.5 mm x 5.5 mm
- 1.0 Volt Core; 2.5 Volt Pad (Tolerant)
- 200 MIPS, 140 BOPS
- 3rd Party IP: ARM 926, AMBA bus, (2) PLLs
- OCP Compliant DSP control bus

Complexity

- 29 million transistors
- > 500 MHz internal clock
- 6 clock domains
- Multiple threshold voltage levels (4)



Demonstration

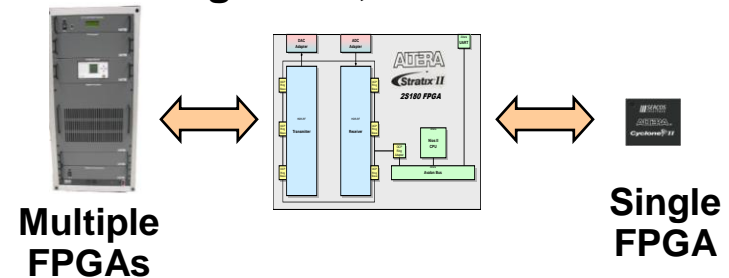
Showcase Impacts

- MITRE's Innovative IC devices
- Highlight Current Capability



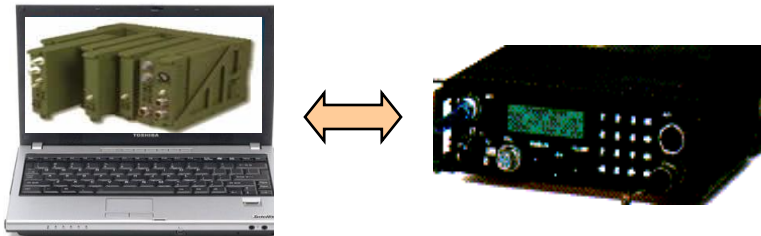
Waveform Reuse Demo

- Demonstrate Waveform Reuse
 - HW agnostic, scalable



JTRS Virtual Radio Demo

- JTRS Virtual Radio voice interoperability with real tactical radio (HW-in-the-loop)



ARM926/SINGARS Demo

- Demo portion of SINGARS port to ARM926 emulation system

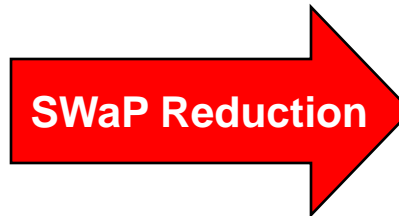


Impacts

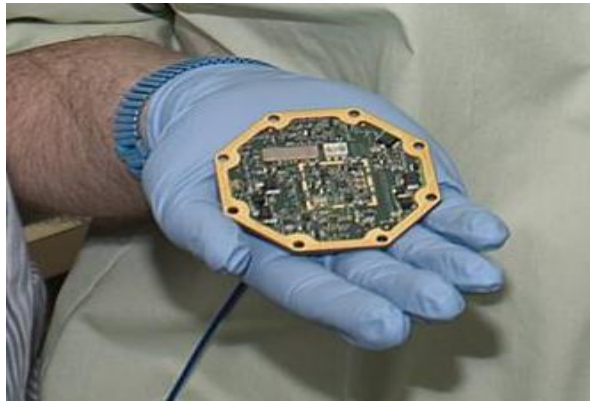


- **This project has enabled MITRE to promote design reuse and portability practices in major acquisition programs**
 - **Air Force FAB-T and HDR-RF, JTRS AMF**
- **The ability to successfully design and deliver next generation Platform SoC designs targeted for our sponsor's applications**
 - **ARM-based 90 nm low power transceiver**
 - **Maintains MITRE's in-depth understanding of advanced semiconductor process and integrated circuit design techniques**
- **Responsible for innovative virtual radio technology currently being used by AMF JTRS to reduce risk in software development and waveform porting**

Future Plans



SINGGARS, SRW



HMS SFF – Black Side Modem

“Double Sided PCB using COTS”

MITRE – Black Side Modem

Low-power single chip solution
Reusable/Scalable HW/SW
Reuses JTRS Waveforms
Significant SWaP reduction
Reduced Cost < \$20 in quantity