Architectures for molecular electronic computers: 3. Design for a memory cell built from molecular electronic devices

Greg Y. Tseng
James C. Ellenbogen

MP 99W0000138
October 1999

MITRE
McLean, Virginia

Architectures for molecular electronic computers: 3. Design for a memory cell built from molecular electronic devices

Greg Y. Tseng
James C. Ellenbogen

MITRE Nanosystems Group

e-mail: nanotech@mitre.org
WWW: http://www.mitre.org/technology/nanotech

MP 99W0000138
October 1999

Sponsor MITRE MSR Program
Project No. 51MSR89G
Dept. W062

ABSTRACT

This paper proposes and explains a design for a digital electronic memory cell that is built solely from molecular electronic devices. The molecular-scale memory cell is modeled after the much larger, micron-scale cell in solid-state nanoelectronic tunneling static random access memory (TSRAM), which has been demonstrated recently. The underlying elements concerning both molecular-scale electronic devices and microelectronic memory architecture are reviewed en route to their synthesis in the design of the molecular electronic TSRAM (i.e., ME-TSRAM) cell. Quantitative theoretical analysis is performed on the proposed ME-TSRAM memory cell, which is a simple planar aromatic molecule measuring only 8 nm by 5 nm. Specifically, *ab initio* quantum mechanical calculations are performed to estimate the capacitances of the various components of the proposed memory cell. On that basis, it is concluded that if it were fabricated, the ME-TSRAM cell would be likely to function as desired. Finally, various fundamental molecular memory cell design issues and architectural challenges are enumerated and discussed. In making and analyzing these specific design proposals for molecular-scale electronic memory, this work attempts to explore the ultimate limits of electronic memory circuit miniaturization.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

I. INTRODUCTION

Complementary to our earlier work on molecular electronic logic [1,2], this paper describes a new design proposal for a nanometer-scale molecular electronic memory cell. The design of the molecular electronic memory cell is analogous to one for a micron-scale quantum-effect memory cell that already has been implemented successfully using more conventional solid-state materials [3-8]. It is described in detail here how such a memory cell might be shrunk drastically in size by implementing it using conductive molecular wires, capacitors, and switches that have been demonstrated in previous experiments [9-21] or proposed in previous theoretical investigations [1,2,22]. This molecular implementation of an electronically addressable information storage cell would have dimensions of only approximately 8 nm by 5 nm. Two variants of this molecular electronic memory cell design are diagrammed in Figure 1.

Based upon this ultrasmall design, quantitative analyses are conducted in Sections III.C and III.D of this work to elucidate the principal structural and operational parameters governing such a molecular electronic memory cell. Particular emphasis is placed here upon understanding and determining (1) the capacitances required to store and read information in the form of one or a few electrons and (2) the switching times required for the memory cell to operate at reasonable speeds. By considering this specific design proposal, one may examine in detail many of the fundamental cell design issues and architectural challenges for ultrasmall molecular-scale electronic memory that also are more broadly applicable.

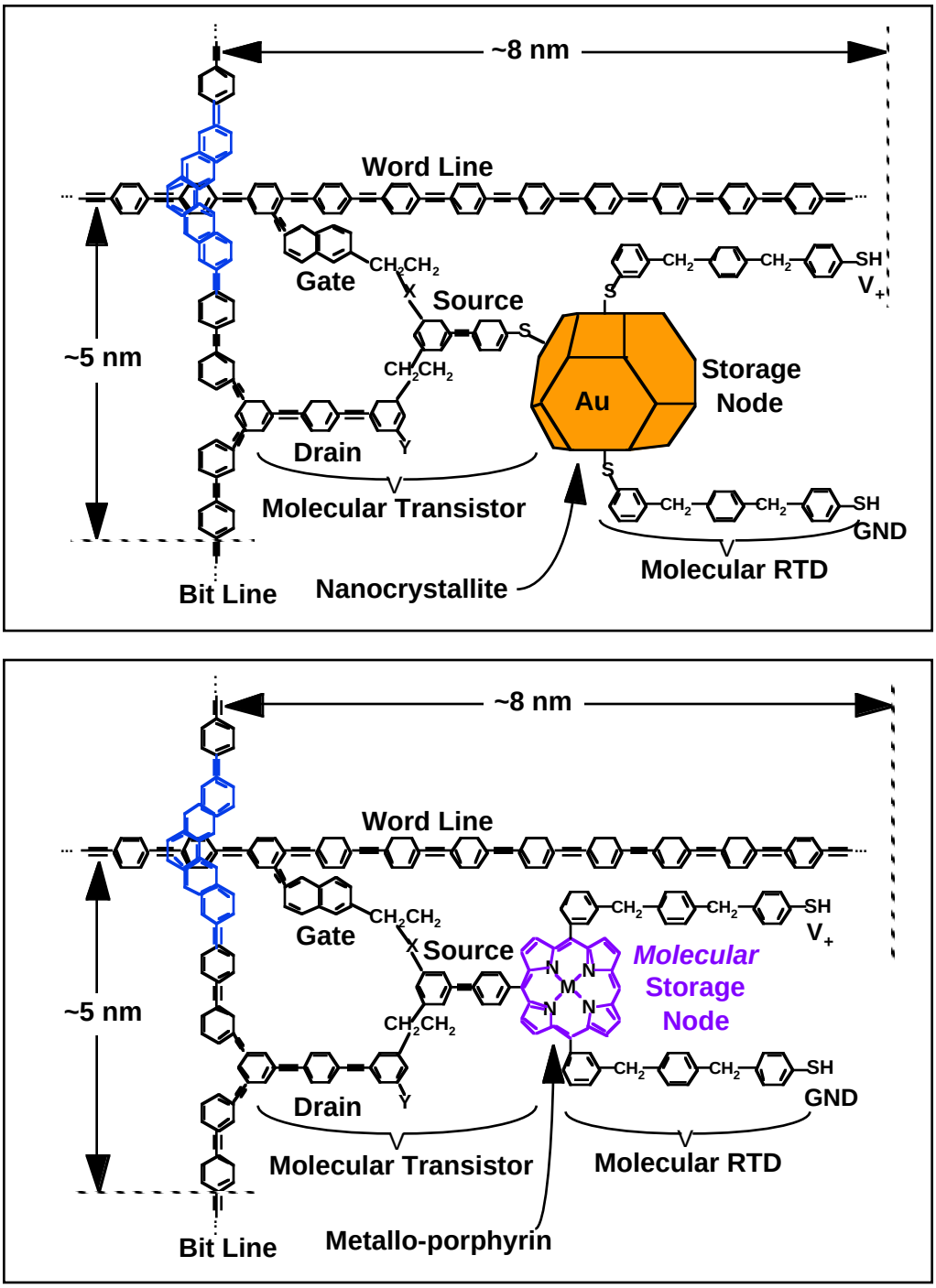
The unprecedented small dimensions of the memory cell design shown in Figure 1 would mean that a regular two-dimensional array of such molecular memory cells should be capable of storing as many as 25 Gigabits of information per square millimeter. This is approximately one million times as dense as digital information can be stored today in conventional solid-state microelectronic memories [23]. In fact, since each component of the memory cell would be a single small molecule, it is reasonable to consider this design as being close to the ultimate in miniaturization for two-dimensional conductive electronic memory. Further, since arrays of these individually addressable molecular electronic memory cells would be planar, with thickness comparable to that of a molecular monolayer, the two-dimensional arrays may be stacked in three dimensions to increase their effective planar storage density even further, without significantly increasing their effective volume. For the reasons outlined above, including the extremely small size of its substituent molecular components, the designs in this work may be considered to be explorations of the ultimate limits of electronic memory circuit miniaturization.

The design strategy is simple for the ultra-small molecular electronic memory cell proposed here. The memory cell is assembled from conductive polyphenylene-based molecular subunits [2], in accordance with the schematic circuit diagram shown in Figure 2(a). This schematic for a quantum-effect nanoelectronic memory cell termed Tunneling-based Static Random Access Memory (TSRAM) originally was developed and demonstrated in amorphous solid semiconductor materials by van der Wagt *et al.* of Raytheon-TI Systems [3-7].

This TSRAM approach is attractive because, as is detailed below, it combines many of the advantages of both conventional Static RAM (SRAM) and Dynamic RAM (DRAM), while avoiding most of their respective disadvantages. The TSRAM design also is particularly attractive amongst various nanoelectronic solid-state memory designs [24-27] that might be implemented more compactly using molecular components. This is because TSRAM contains only components for which molecular analogs have been demonstrated or proposed, and, especially, TSRAM relies in its operation upon quantum effects that readily occur in these known conductive molecular devices.

Thus, these molecular devices or subunits that were developed in earlier work are assembled in the molecular electronic TSRAM (ME-TSRAM) structures shown in Figure 1 in accordance with the general TSRAM schematic of Figure 2(a). These molecular electronic devices include molecular wires fabricated by Tour *et al.* [9,10,12,13], then demonstrated by Weiss *et al.* [14]. A gold nanocrystallite, demonstrated by Reifenberger *et al.* [20,21], is employed as a capacitor in the molecular electronic memory cell implementation proposed in Figure 1(a). Purely molecular porphyrinic alternatives also are considered for use as a capacitor or bit storage node. Finally, the component devices include two-terminal molecular resonant-tunneling diode switches that recently have been synthesized by Tour *et al.* [10,13] and demonstrated by Reed *et al.* [19,28,29], plus three-terminal molecular electronic resonant-tunneling transistor switches proposed by Ellenbogen [2].

Below, in Section III, the specifics of the ME-TSRAM design proposal are presented, and quantitative analyses of this proposal's principal structural and operational parameters (capacitance



NOTE: X = Electron donating group (e.g., OCH, CH_3); Y = Electron accepting group (e.g., CF_3, CN); M = Metal atom (e.g., Mg, Mn, Cu, Fe, etc.)

Figure 1

Designs for a Tunneling-based Static Random Access Memory (TSRAM) cell which is implemented with molecular electronic devices and includes as the storage node (a) a gold nanocrystallite and (b) a porphyrin molecule

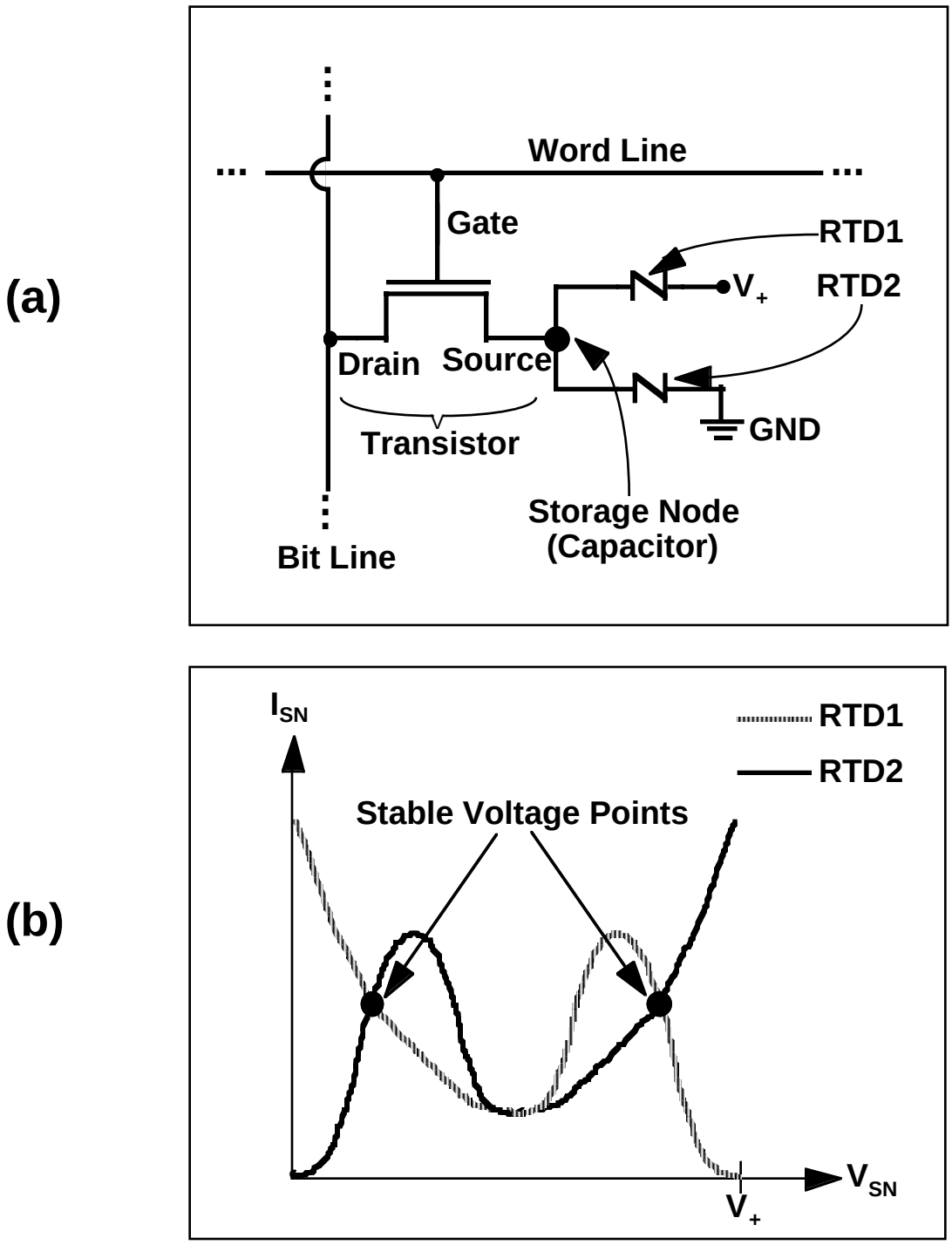


Figure 2

Tunneling-based Static Random Access Memory (TSRAM): (a) Schematic circuit of Raytheon-TI design for a TSRAM cell and (b) current-voltage (I-V) characteristics at the storage node (SN); note the two stable points. Adapted from [6];

and switching times) are performed. In Section IV various other fundamental cell design issues and architectural challenges are enumerated and discussed. First, however, in Section II.A we provide background on the essential elements of molecular electronics that underlie this proposed molecular electronic implementation of a memory design borrowed from solid-state nanoelectronics. Then, in Section II.B we describe the basic principles of microelectronic memory, some of which are manifested in the nanoelectronic TSRAM design as described in Section II.C.

II. BACKGROUND

Molecular electronics is an approach for drastically decreasing the size and increasing the density of electronic circuits by building them from wires and switches that consist of individual covalently bonded molecules [1,30,31]. Proposals for molecular electronic devices and systems date back to the seminal work of Aviram and Ratner in 1974 [22]. Only recently, however, have experimental results and associated theoretical analysis demonstrated that small molecules have electrical properties which seem to make them appropriate for use in building electrically conductive devices and circuits [19,32-37].

Presently, there are two primary types of small molecules that have been proposed and demonstrated for use in molecular electronic circuits. These two types of molecular backbones are: (a) polyphenylene chains [1,2,29], and (b) carbon nanotubes [38-46]. A number of the design considerations outlined here for polyphenylene-based molecular memory circuits also would apply to molecular memories built from carbon nanotubes or other molecular-scale structures. However, only the polyphenylene-based molecular components will be reviewed here because our proposal for molecular electronic memory is polyphenylene-based. In particular, developments in regard to five types of molecular electronic components, which have been reviewed more extensively elsewhere [1], will be discussed here in brief: wires; rectifying diodes; resonant-tunneling diodes; resonant-tunneling transistors; and gold nanocrystallites.

A. Polyphenylene-based molecular electronic devices

1. Molecular wires. An exciting recent development in molecular electronics is the demonstration of the most basic polyphenylene-based electronic device: the "Tour wire" [9,10,12,13]. In 1996, after extensive theoretical research [12,47-50], these chains of organic aromatic benzene rings were shown experimentally to conduct small electrical currents like wires [14,20]. A Tour wire is illustrated in part (a) of Figure 3. Previously, Tour *et al*. refined the synthetic techniques for conductive polyphenylene chains (molecular wires) by developing precise synthetic methods that produce enormous numbers of these molecules (~10^{23}), every one of which is of exactly the same structure and length [11,12,51].

2. Molecular rectifying diodes. Another recent experimental development is the demonstration of molecular electronic rectifying diodes or "molecular rectifiers" [15-18], which are similar to those proposed by Aviram and Ratner in the first scientific paper on molecular electronics [22]. A typical molecular rectifier, as depicted in Figure 3(b), introduces electron acceptor and donor substituents into benzene ring-based structures so that it becomes more difficult to conduct electrical current in the reverse direction than in the forward direction (i.e., a much larger reverse bias voltage than forward bias voltage is required to conduct current). To extend these developments further, efforts are underway to propose and characterize polyphenylene-based rectifiers which should be more appropriate in structure for building digital circuitry with a backbone of Tour wires [1,33].

3. Molecular resonant-tunneling diodes. Alongside the progress of rectifying diodes, molecular electronic resonant-tunneling diodes (RTDs) have been synthesized and demonstrated recently. Shown in Figure 3(c) is a diagram of a molecular RTD that has only very recently been synthesized by Tour [10,13] and demonstrated by Reed [19,28,29]. Structurally and functionally, this device is simply a molecular analog of the much larger solid-state RTD [31]. The RTD operates upon the physical principle that electrons can tunnel quantum mechanically through a barrier when the energy of the incident electrons is in alignment with one of the quantized energy levels on a narrow “island” between two barriers to electron tunneling. In an RTD, the bias voltages can be adjusted to shift the energy levels of the island in and out of alignment with the energy of the incident electrons. Since there are multiple energy levels in the barrier, there are actually multiple "on" and "off" states for an RTD. Such characteristics exemplify the new possibilities in electronic circuit design made possible by devices which operate upon quantum effects. This has been and will continue to be important and advantageous in the design of extended nanoelectronic solid-state [52,53] and molecular [1,2] circuitry. However, one crucial fact about diodes, whether micro-, nano-, or molecular

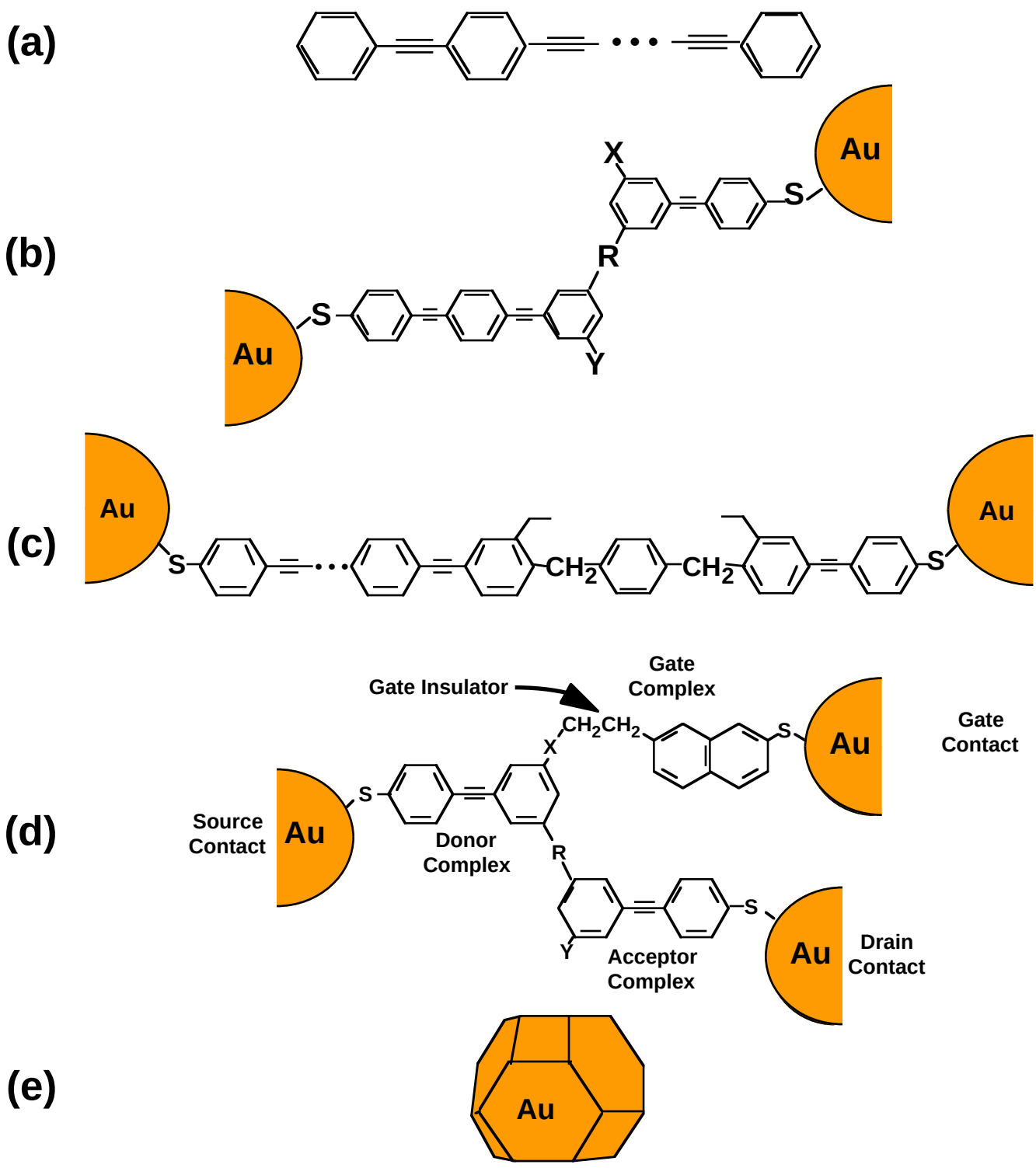


Figure 3

Diagrams of various molecular electronic devices: (a) Tour wire; (b) rectifying diode; (c) resonant-tunneling diode (RTD); (d) resonant-tunneling transistor (RTT); and (e) gold nanocrystallite;

electronic, still remains: there is no amplification (or "gain") of voltage.

4. Molecular resonant-tunneling transistors. To achieve gain in a switching device, a three-terminal switch or "triode" is required. Though they have not been synthesized or demonstrated, various flavors of resonant-tunneling transistors (RTTs), three-terminal devices with the ability to produce gain, have been conceptualized [2]. A typical molecular RTT, as diagrammed in Figure 3(d), operates on the same physical principle of quantum tunneling as the RTD. However, in the RTT, the shifting of the energy levels in the tunnel barrier is controlled by the voltage on the third "gate" terminal, not by the bias voltage. In this scheme, a small gate voltage modulates a much larger source-drain bias voltage; hence, the RTT exhibits gain. Therefore, the RTT is a crucial element in designing circuits which require amplification [2].

5. Gold nanocrystallites. In recent years, researchers have succeeded in refining methods to synthesize nanometer-scale clusters of gold atoms and adsorb them to molecules for the storage of charge and other uses [20,21]. One such cluster is depicted in Figure 3(e). Although such clusters are not polyphenylene-based, as are the other molecular circuit components discussed here, they are of the same scale and have very desirable properties complementary to those of the polyphenylenes, especially for molecular electronic memories.

Developments in polyphenylene-based molecular electronics such as those discussed above suggest that it may be possible to fabricate extended electronic circuits out of molecules. Research in extended circuitry is in progress and advances have been made in designing logic circuits [1,2]. To drive the development of molecular circuitry into the realm of memory, it is necessary first to review the basic principles of microelectronic memory.

B. Basic principles of microelectronic memory

Although data may be stored in a variety of devices, in this section, the term "memory" is taken to refer only to fast electronically addressable digital information storage, usually random access memory (RAM) with no moving mechanical parts [54]. Here, we outline defining characteristics of electronic memory and then discuss in more detail basic principles of three classes of conventional microelectronic memory.

Data is stored in digital electronic memories as arrays of bits, each of which has the value one or zero. All electronically addressable memory consists of memory "cells," each of which stores one bit. In general, a memory cell has two requirements: (1) that its state can be changed to represent a one or a zero and (2) that its state can be sensed. There are a number of arrangements of linked electronically controlled switches (and other devices) that satisfy these requirements.

Electronically addressable memory falls into two broad categories, read only memory (ROM) and random access memory (RAM). RAM is further subdivided into dynamic RAM (DRAM) and static RAM (SRAM). The conventional microelectronic variants of these three classes of memory—ROM, DRAM, and SRAM—share a number of similar features. Figure 4 compares the structures of these three classes of microelectronic memory. Observe that they all consist of regular arrays of individual memory cells connected to other cells by a two-dimensional lattice of wires. Each cell contains at least one transistor-like switch, as indicated by the presence in Figures 4(a)-(c) of the three-terminal schematic symbol for a transistor. The main difference between these classes of memory is in the structures of their respective memory cells. The structural differences give each class of memory distinctive capabilities, as well as distinctive operational approaches to storing and accessing information.

ROM cells, as shown in Figure 4(a), store logical ones and zeros as disabled transistors (those that have been "written" by deactivating them) and enabled transistors (those that still can be activated), respectively. This structure makes read-only memory unalterable—i.e., the bits cannot be changed. It is also "nonvolatile"—i.e., the bits remain intact even when the power is turned off [55].

In contrast, RAM is alterable and volatile. That is, the memory supports both read and write operations, but it loses its contents when the power is turned off. Each DRAM cell shown in Figure 4(b) consists primarily of a tiny capacitor on which charge is stored to represent a bit. However, this charge normally dissipates within milliseconds, so DRAM requires a mechanism for periodically refreshing stored charges.

The SRAM cell diagrammed in Figure 4(c) is a "flip-flop," a logic structure constructed from the six transistors connected by the combination of bar-like and cross-like wires. (Sometimes electrical engineers refer to this structure as "cross-coupled inverters.") Inherent in this logic structure is the continuous feedback of signals that allows logical

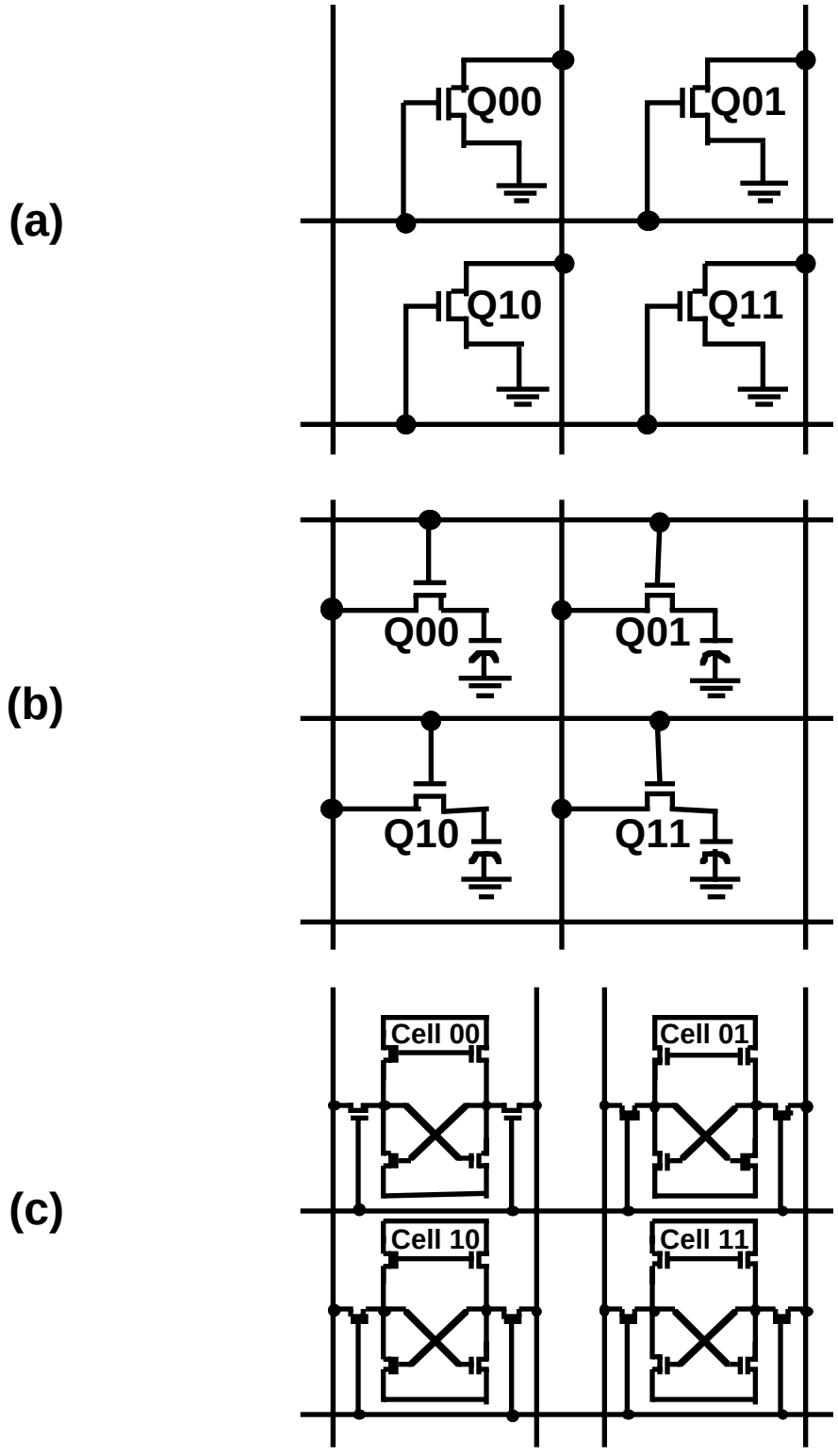


Figure 4

Schematic circuits for 2 by 2 cell lattices of three classes of microelectronic memory: (a) Read Only Memory (ROM); (b) Dynamic Random Access Memory (DRAM); and (c) Static Random Access Memory (SRAM);

ones and zeros to be stored indefinitely, or at least until the power is turned off.

In comparing these two classes of RAM, we note that SRAM is faster and requires less power, because its gate transistors are optimized for speed and its operation does not require a refresh. DRAM has the advantage of being denser because it requires fewer components, but it is slower and consumes more power because each cell requires refreshing periodically [54-57]. Thus, DRAM and SRAM each have significant advantages and disadvantages.

C. Tunneling-based SRAM

The advantages of both conventional DRAM and SRAM are incorporated in the new Tunneling-based SRAM or TSRAM cell. Researchers at Raytheon-TI have developed and tested this novel "hybrid" approach to memory design, which uses both microelectronic and nanoelectronic devices [3-7]. It is because the TSRAM exploits the unique properties of quantum-effect nanoelectronic devices that it is able to combine the advantages of DRAM and SRAM.

Observe in Figure 2(a) that the TSRAM cell is structurally similar to DRAM. The difference is the addition of a pair of RTDs that together make an "RTD latch" coupled to the storage node. Note that the voltage at the storage node V_{SN} determines the bias voltages across both RTDs in the latch. Because of this and the peak-valley current-voltage characteristics of an RTD, this latch maintains only two stable voltages at the storage node [4,5], as depicted in Figure 2(b). These two stable voltages, corresponding to high or low charge on the storage node, are taken to represent a one or a zero, respectively. This allows a TSRAM cell, consisting of only one transistor, two RTDs, and a capacitive element, to store a bit statically (i.e., without global refresh as in DRAM) [6]. To write or read a bit, the gate is charged, allowing the phenomenon of charge sharing to alter selectively the voltage on the bit line and the storage node.

Here we consider primarily the details for the read operation, since those set the lower bound on the capacitance that the molecular-scale storage node must have in order for the cell to function. This is of interest because it is not a given that a small molecular structure will have sufficient capacitance to store information in the form of additional electric charge.

During the read operation, if the cell was in the one state, then the bit line voltage is altered measurably; and if the cell was in the zero state, then the bit line voltage remains unchanged. In either case, after charge sharing (explained in more mathematical detail in Section III.B.1) the cell will be in the zero state. Hence, refresh after readout is required, although global periodic refresh is not. Thus, TSRAM encompasses the advantages inherent in both the operation of SRAM and the structure of DRAM.

Due to its relatively simple structure, a solid-state TSRAM cell occupies only ~150 mm^2 in area, which is significantly smaller than a standard solid-state microelectronic SRAM cell, though somewhat larger than a standard DRAM cell, as expected [6]. Also, the static operation of TSRAM requires much less power than conventional memories, and it is very fast. SPICE modeling predicts sub-nanosecond access times [6]. Since the TSRAM offers these many advantages, and a 16-cell system has been tested in solids, we choose to utilize this design as the basis for our proposed molecular electronic memory design. It seems likely that the quantum effects upon which the TSRAM cell relies would be readily adapted and even enhanced [58] by assembling such a memory cell from ultrasmall molecular components.

III. MOLECULAR ELECTRONIC MEMORY CELL

A. Design

We combine the above-described developments in molecular electronic devices with the solid-state TSRAM design to propose molecular electronic implementations of TSRAM or ME-TSRAM, as diagrammed in Figure 1. In Figure 1(a), observe that the various elements of the TSRAM design are built from molecules. These molecules serve in the roles of the wires, RTDs, and transistor needed to implement the memory cell circuit described in the schematic in Figure 2. Further, a gold nanocrystallite serves as a capacitive storage node for one or a few electrons. Of the several variants of molecular transistors, an enhancement mode ME-RTT [2] is chosen to serve as the three-terminal switching element in the ME-TSRAM cell because it is most similar in function to the three-terminal switching element employed in the demonstrated solid-state TSRAM. An enhancement-mode ME-RTT is one that is "off" (i.e., current is blocked from flowing through it) when there is no voltage applied to the gate and is turned "on" (i.e., current is allowed to flow through it) by a voltage applied to the gate, just as is required of a solid-state transistor in a similar role.

It is noteworthy that the molecular electronic memory cell diagrammed in Figure 1(a) would measure only about 8 nm by 5 nm, which is more than one million times smaller in area than the corresponding solid-state TSRAM cell. In fact, it may be reasonable to consider the present design as being the ultimate in miniaturization for conductive electronic memory, or very close to that limit. This and other advantages of ME-TSRAM are summarized in Table 1, which compares the various types of electronic memory that have been discussed above. In Table 1, a check (**3**) refers to an advantage while an "X" (**5**) refers to a disadvantage. Note that all three features--speed, power, and, especially, size--are advantages of ME-TSRAM.

To illustrate explicitly the size advantage and provide further comparison, we present in Table 2 the area per bit for current standard microelectronic memories [23], emerging solid-state nanoelectronic memory [6], and projected microelectronic memories [23] alongside our estimated size for the proposed molecular electronic memory. It is significant to note that a *molecular* TSRAM with bit area of ~40 nm^2 could be over one million times smaller than its *solid-state* nanoelectronic counterpart, the "hybrid" TSRAM with a bit area of 1.5×10^8 nm^2. Additionally, it is significant to note that the ME-TSRAM bit area still would be over one thousand times smaller than the bit area of 5.5×10^4 nm^2 projected for DRAM in the year 2007.

The ME-TSRAM derives its size advantage in part from the fact that it proposes to represent a bit by storing one or a few electrons on the gold nanocrystallite. However, this type of storage node prevents the memory cell from being purely molecular. This goes beyond an issue of nomenclature: it presents an issue for the synthesis of the memory cell. To fabricate the structure in Figure 1(a), the molecules surrounding the gold cluster would be adsorbed, not covalently bonded, to it. This could introduce a synthesis problem because memory cells must be produced by the trillions. This feat is likely to be routine for a purely molecular cell [11,51], but arduous for one with disparate types of molecular-scale components. Thus, it would be advantageous if the memory cell were to consist of only covalently bonded molecular subunits. It is desirable, therefore, to consider replacing the experimentally studied gold nanocrystallite with a sort of "molecular capacitor."

Specifically, we consider replacing the gold nanocrystallite with a porphyrin molecule as the storage node of the memory cell design in Figure 1(a). Observe in Figure 1(b) the insertion into the ME-TSRAM cell of this candidate for a molecular capacitor results in a design for a *purely molecular* electronic memory cell. It is reasonable to consider a porphyrin molecule as a molecular capacitor because it may be inferred from experiments that such molecules have a sufficiently high "capacitance," just as is required in storage nodes for larger microelectronic memory cells [59-60].

Porphyrins constitute a family of molecules, commonly found in nature. The structure of each porphyrin molecule is a large macrocyclic ring of twenty carbon atoms and four nitrogen atoms with perhaps a metal atom bound in the center [60], such as is shown in Figure 1(b). These molecules, examples of which are hemoglobin and chlorophyll, are known to be "reaction centers" in charge transfer reactions, such as those which occur in photosynthesis. Implicit in charge transfer, the acceptance and donation of charge, is the storage of charge. Noting this, we may plausibly infer that a porphyrin molecule is a kind of molecular capacitor. Other candidates for molecular capacitors include the fullerenes C_{60} and C_{70}, which have been discussed elsewhere in connection with molecular electronics [39].

Thus, to examine the efficacy of various candidates for a molecular storage node, and hence to analyze the key element of the ME-TSRAM, we must consider their capacitances in a more quantitative manner. This will also give insight to the RC time constant, which is a measure of switching time for the memory cell. However, before determining whether the various candidates for a molecular storage node meet the requirements of capacitance and switching times, we need first to estimate the requirements of such parameters.

B. Requirements upon structural and operational parameters

1. Capacitance. There are two requirements that set the lower bounds on the capacitance needed in the molecular electronic storage node. The first requirement is absolute and fundamental, while the second is relative and practical.

In accordance with the relation involving capacitance $Q = CV$, a fundamental lower bound on the capacitance C would be 0.020 aF, corresponding to maximum potential V of 8 volts being applied to store a charge Q equivalent to one electron. This capacitance is an absolute lower limit for the storage node, because a voltage greater than approximately 8 volts may dissociate or ionize various parts of the molecular memory cell.

Features

Design	Speed	Power	Size
DRAM	× Slow periodic refresh is required	× Inefficient periodic refresh is required	✓ Small uses two devices
SRAM	✓ Fast refresh never required	✓ Efficient refresh never required	× Large uses six devices
TSRAM	✓ Fast periodic refresh not required	✓ Efficient periodic refresh not required	✓ Small-Med DRAM + 2RTDs
ME-TSRAM	✓ Fast periodic refresh not required	✓ Efficient periodic refresh not required	✓✓ Very Small built from molecules

NOTE: ✓ = advantage; × = disadvantage.

Table 1

Comparison of various features of the DRAM, SRAM, TSRAM, and ME-TSRAM designs

Solid-state

Type of Memory	Status	Area per bit (nm^2)
MITRE *Molecular* Electronic Memory (MITRE projected)	Designed	~40
4Mb SRAM Standard	COTS*	6.0×10^8
64Mb DRAM Standard	COTS	3.0×10^6
"Hybrid" TSRAM	Tested	1.5×10^8
DRAM (projected via SIA Roadmap)	Year 2004 Year 2007	1.55×10^5 5.5×10^4

NOTE: COTS = Commercial Off The Shelf

Table 2

Area per bit for standard, emerging, and projected solid-state electronic memories and projected area per bit for proposed molecular electronic memory (all values are in units of square nanometers)

Defining the other, practical requirement necessitates some further discussion about the charge sharing that must occur before and during the read operation. Before a cell is read, the transistor is "off," and hence the bit line (BL) and storage node (SN) are electrically separated. In this case, the total charge Q_I initially on the bit line and storage node is the sum of their respective charges:

$$Q_I = Q_{BL} + Q_{SN} = C_{BL}V_{BL} + C_{BL}V_{SN},$$

where C_{BL} and C_{SN} are the capacitances on those two structures, respectively, and V_{BL} and V_{SN} are the corresponding voltages. During the read operation, the transistor is "on," and hence the bit line and storage node are electrically connected. The electrical connection forces the bit line and storage node to share charge in order to equilibrate to a final voltage. Thus, the total final charge Q_F is given by

$$Q_F = (C_{BL} + C_{SN})V_F,$$

where V_F is the final voltage of the storage node and of the bit line. Conservation of charge requires

$$Q_I = Q_F \Rightarrow V_F = \frac{C_{BL}V_{BL} + C_{SN}V_{SN}}{C_{BL} + C_{SN}}.$$

The quantity that is measured in reading the state of the node is $\Delta V = V_F - V_{BL}$, which can be expressed as

$$\Delta V = V_F - V_{BL} = \frac{V_{SN} - V_{BL}}{C_{BL}/C_{SN} + 1}.$$

Typically, before the read operation, the bit line is charged to the storage node voltage for state zero. Thus, for state zero, charge sharing would effect no change on the bit line voltage ($\Delta V = 0$), whereas for state one (with higher voltage than state zero), charge sharing would effect a positive ΔV. The extent to which this change in bit line voltage is measurable is related directly to the denominator of ΔV. Specifically, the "transfer ratio" C_{SN}/C_{BL} must be at least 0.1. This serves to keep the value of ΔV above the thermal noise threshold of approximately 0.025 volts for sensing a charge of one electron at room temperature [61]. The transfer ratio establishes a lower limit on the storage node capacitance with respect to the bit line capacitance.

Thus, to assess the efficacy of various storage node candidates, we must also calculate the capacitance of the bit line, which in the designs of Figure 1 is specified to be an approximately 10-benzene long Tour wire. Initial quantum calculations to determine C_{BL} and other quantities have been conducted by the authors, and they are presented and discussed below in the next section.

2. Switching times. When the molecular transistor is turned "on," it provides a *resistive* electrical connection between the bit line and the storage node. As we will show, this resistance, along with the capacitance of the storage node, provides a measure of the switching time for the memory cell circuit. The RC time constant t is a measure of switching time and, for the TSRAM, it is determined by R_{on}, the resistance of the molecular transistor when turned on, and the series combination of C_{BL} and C_{SN}:

$$\tau = R_{on}\frac{C_{SN}C_{BL}}{C_{SN} + C_{BL}} = R_{on}\frac{C_{SN}}{C_{SN}/C_{BL} + 1}.$$

If we assume C_{SN}/C_{BL} is ~0.1, as was established above, then the denominator in t is approximately unity. To a good approximation, then,

$$\tau \cong R_{on}C_{SN}.$$

Here, one can verify that t has units of time simply by noting that R has units of volt/amp and C has units of charge/volt:

$$[\tau] = [R][C] = \frac{\text{volt}}{\text{amp}} \cdot \frac{\text{coulomb}}{\text{volt}} = \frac{\text{coulomb}}{\text{amp}} = [\text{time}].$$

A useful point of reference for switching times is a time on the order of 1 nanosecond (ns), which corresponds to that of state-of-the-art electronic computers operating at or around 1 Gigahertz (GHz), or 1000 Megahertz (MHz). Although it is likely that molecular circuits will be useful even if they operate slower than conventional microelectronic circuits [1], it is nonetheless reasonable to ask what we must require if we wish molecular circuits to operate as fast as state-of-the-art microelectronic circuits.

C. Calculation of capacitance

Calculating the capacitance of the various storage node candidates requires a method by which to model generally and quantitatively the capacitive nature of atomic- and molecular-scale structures. For this purpose, we employ a previously developed formalism on the capacitive nature of atomic-sized structures [62]. At the atomic scale, the concept of capacitance becomes considerably more involved than that of a constant electrostatic capacitance [63].

The capacitance of macroscopic and micron-scale structure is a function of only its geometry and

material properties. Especially, this bulk capacitance is independent of the net charge on the system. However, the capacitance of an atom or a molecule has an explicit dependence on the net charge. This is because of the relatively small number of electrons in an atom or molecule and because of the way quantum effects dominate the addition or removal of charge in structures on the scale of atoms and molecules [62-64].

Nonetheless, even on the nanometer scale, the qualitative notion of capacitance as the ability (i.e., the "capacity") to store charge still is valid despite the complexities that must be addressed when considering from a quantum mechanical viewpoint the design constraints upon the memory cell proposed here.

In their 1995 paper [62], Iafrate *et al.* derived a formula for the capacitance *C(N)* of a closed *N*-electron system. This was achieved by using the chemical potential to derive the following connection among the ionization potential, the electron affinity, and the capacitive energy:

$$\frac{e^2}{C(N)} = I(N) - A(N) \Leftrightarrow C(N) = \frac{e^2}{I(N) - A(N)}.$$

Above, *I(N)* and *A(N)* are the ionization potential and the electron affinity of the *N*-electron system, respectively, and *e* is the fundamental unit of charge. Their methods first were applied to computational models of quantum dots, which yielded the expected periodicity of addition energy versus electron number [63,64]. Further, they showed that the results from the statistical mechanical formula above approaches classical results from electrostatics as the number of electrons *N* gets large [62].

Thus, from knowledge of the ionization energy and electron affinity of a molecule, we may calculate its capacitance. However, Iafrate's formula is exact only when it is applied to closed, isolated systems, which are systems that do not couple to any other systems. From a mathematical standpoint, closed systems release electrons to an infinite distance away and also receive electrons from an infinite distance. This is not the case for a molecular storage node since it interacts with other nearby structures, such as the bit line. A more complete description of our system would include terms for the interactions between the storage node and all structures with which it interacts. But, for the purposes of this paper, we employ the closed system approximation since preliminary analysis indicates that the interaction terms will increase the capacitance [65]. Thus, if our calculations under the closed system approximation indicate that a molecular storage node has sufficient capacitance, then calculations that include interaction terms also should give the same affirmative conclusion.

To calculate the capacitance of the bit line and various storage node candidates under the closed system approximation, we employed the Spartan [66] and Gaussian [67] molecular modeling software packages to perform *ab initio* quantum mechanical calculations of the quantities that appear in Iafrate's formula. In these calculations, the quantity of interest is the ionization energy *I* minus the electron affinity *A*, or *I – A*. Employing *ab initio* methods to determine the total energies of the neutral ground state *N*-electron system, as well as the ground state (*N – 1*)-electron cation and the ground state (*N + 1*)-electron anion, the ionization potential and the electron affinity for the neutral system are readily calculated from their definitions, as follows [62]:

$$I(N) = E(N-1) - E(N)$$
$$A(N) = E(N) - E(N+1),$$

where *E(j)* refers to the ground state energy of the *j*-electron system. Thus, the quantity in which we are interested can be written as

$$I(N) - A(N) = E(N+1) - 2E(N) + E(N-1) \cong \left[\frac{\partial^2 E(j)}{\partial j^2}\right],$$

evaluated at $j = N$. Observe also that the energetic quantity of interest is a kind of finite difference formula that approximates the second derivative of the energy with respect to the variation in the charge number.

Capacitances were estimated for the key molecular components of the ME-TSRAM cell according to the formulas above. In cases where the values for *I(N)* and *A(N)* were not known from experiment, the energies *E(j)* were calculated using *ab initio* Hartree-Fock methods with basis set 6-31G* [66-67]. For molecules that did have experimentally measured ionization energies and electron affinities, we simply used those values without performing the somewhat time consuming computations demanded by the Hartree-Fock method. A summary is presented in Table 3 of all the capacitances thus determined for molecules relevant to this study.

Several observations can be made from these results, using the ideas introduced in Section III.B.1. First, from a consideration on the practical lower limit on the capacitance and assuming, therefore, that the transfer ratio is 0.1, the calculation that a 10-benzene Tour wire bit line has capacitance 0.018 aF establishes a lower limit of 0.0018 aF on the

Molecule	I (eV)	A (eV)	I - A	C (aF)
10-benzene Tour wire*	5.25	-3.83	9.08	0.018
Porphyrin (naked)**	4.30	0.50	3.79	0.042
Mg-porphyrin**	4.46	0.67	3.80	0.042
Fe-porphyrin*	9.98	0.33	9.65	0.017
C_{60}***	7.58	2.65	4.93	0.032
C_{70}***	7.61	2.72	4.89	0.032

NOTE: * Quantities calculated via Spartan quantum chemistry software package [66]
** Quantities calculated via Gaussian quantum chemistry software package [67]
*** Quantities experimentally measured, as tabulated in [39]

Table 3

Calculations of capacitance for bit line and various candidates for storage node in ME-TSRAM

capacitance for the storage node. Comparing this with the larger fundamental lower limit of 0.020 aF given in Section III.B.1, it is seen that a capacitance of at least 0.020 aF is required for the storage node to be effective in this ME-TSRAM design. Table 3 indicates that four of the five candidates—naked porphyrin, Mg-porphyrin, C_{60}, and C_{70}—satisfy this requirement, while the Fe-porphyrin does not.

D. Calculation of switching times

For an order-of-magnitude estimate of the RC time constant we need only two pieces of data, namely R_{on} and C_{SN}. Recent experiments have shown that polyphenylene-based structures, such as transistor in the ME-TSRAM, have a resistance on the order of 10^7 ohm [36]; hence $R_{on} \sim 10^7$ ohm. Our calculations have determined C_{SN} to be on the order of 10^{-20} F. Thus, we expect switching time of ME-TSRAM to be of order 10^{-13} or 10^{-12} s, which is far less than the upper limit of 1 ns or 10^{-9} s. This provides an encouraging order-of-magnitude estimation. It is necessary to observe, however, that measurements of the current through a polyphenylene-based wire suggest that the current may only be approximately 10^{11} electrons per second [1], which does not seem to be large enough to sustain such fast switching times. A more sophisticated formalism for the RC time constant of a molecule, which takes into account Landauer conductance [68] and other factors, presently is being developed [69].

IV. DISCUSSION

The preceding section presented a design for molecular electronic memory and provided computational results and analysis supporting its structural and operational efficacy. However, it is clear that many other issues and challenges must be addressed before molecular electronic memory can be realized in the form proposed here or in some other form. Thus, this section is devoted to enumerating and to discussing some of these fundamental cell design issues and architectural challenges.

A. Fundamental cell design issues

Fundamental design issues are those that one must consider in order to design individual molecular-scale digital electronic memory cells that will perform as desired. This requires designing a cell that possesses two stable states such that (1) the state can be changed to represent a one or a zero and (2) the state can be sensed. In this connection, many issues arise when memory cell circuits are extended down to the molecular scale. These can be addressed by various analytic and computational modeling techniques, but experiments are likely to be required also to answer them definitively. The issues enumerated and discussed below apply to the ME-TSRAM cell, but likely are more broadly applicable, as well.

1. Combining individual devices. In the implementation of TSRAM in molecules, we have assumed implicitly that individual molecular electronic devices (wires, switches, and capacitors) can be bonded or "wired" together to create a circuit that is the "sum of its parts." By this it is meant that the behavior of the entire circuit is defined simply by the combination of the electrical properties of its individual components. This is true to an extremely good approximation in micron-scale solid-state circuit design, but it is likely that it is a much poorer approximation for molecular circuits. Because molecules operate in the quantum mechanical domain, when molecular-scale devices are combined to form large molecular circuits, these components cannot be expected to behave in the same way they do in isolation. This is discussed in further detail elsewhere [1].

2. Charge sharing. Due to the issue mentioned above regarding combinations of individual devices, there is reason to question how or if the phenomenon of charge sharing extends down to the molecular scale. That is, experiments have shown that the equations detailed in Section III.B.1 apply in extremely good approximation to micron-scale solid-state circuits. However, because of quantum wave interference and other effects that influence the molecular charge distribution, these equations may not apply as well to molecular electronic circuits.

3. Stabilization of bit state. The operation of the ME-TSRAM as a molecular analog of solid-state TSRAM requires establishing a bistable voltage for the storage node. As indicated in Figure 2(b), the voltages are stabilized by a continual small current that flows from V_+ to ground. However, the capacitance calculations detailed in Section III.C suggest that only one or a few electrons are stored on the storage node at any given time. Thus, the current from V_+ to ground in the ME-TSRAM may be very small. If the current is too small, it may be difficult to stabilize the voltage V_{SN}.

4. Mechanisms of conductance. Strongly coupled to all the issues discussed above is the issue of how electrons are conducted through polyphenylene-based molecules. This conduction likely occurs via a multiplicity of mechanisms in small molecules. Most of these molecular conduction

mechanisms are different from those that dominate conduction in micron-scale metallic wires. This presents a significant design issue because different mechanisms may dominate at different scales (e.g., device scale vs. circuit scale). This issue also is discussed in greater detail elsewhere [1].

B. Architectural challenges

In addition to the design issues that primarily affect individual memory cells, there are architectural challenges that would affect the super-aggregations of cells that must be present in an extended molecular electronic memory. The challenges enumerated and discussed below apply to the ME-TSRAM architecture, a two-dimensional lattice of cells, but likely are more broadly applicable, as well.

1. Energy dissipation. As electrons travel through a molecule, some of their energy can be transferred to motions of the nuclei in the molecule, such as the internal vibrations and rotations. The amount of energy transferred is dependent on how strongly the electronic energy levels of the molecule couple to the vibrational modes of the molecule. This dissipation of energy, therefore, varies with the different mechanisms of conductance discussed above. Energy dissipation is an architectural issue for any molecular memory proposal because it will diminish the effectiveness of electron transport and signal transmission through a molecular structure. In the extreme case, it could lead to the breaking of bonds and the destruction of the device. Dissipation is discussed in further detail elsewhere [1].

2. Addressing. A challenge for molecular-scale architectures is the problem of addressing individual molecular memory cells. This problem is sometimes posed as the problem of connecting the functional molecular devices to "the outside world." That is, while molecular electronics proposes to use molecules to compute and store data, the molecules must be interfaced with structures with which a user may interact for input and output (I/O) purposes. In recent experiments on single-molecule conductivity [36,42], these interface structures typically have been nanometer- or micron-scale metallic contacts (e.g., gold, platinum) that make poor electrical contact with the molecules. The experimental setup generally consists of a molecule sandwiched between two much larger contacts or of a long molecule placed upon up to seven larger electrodes [70]. If the addressing of a molecular memory architecture were simply to extend this approach, it would require perhaps on the order of one million electrodes, one placed every ten nanometers. Not only would this present an extremely arduous assembly problem, but the close mutual proximity of the electrodes likely would induce mutual interference or crosstalk, corrupting the signals. Thus, an effective method of addressing must overcome the general challenges of assembly and signal integrity, in addition to others that may arise in specific cases.

3. Chemical assembly and defect tolerance. As indicated above, chemical synthesis of molecular electronic devices is highly advantageous because it can produce rapidly and economically enormous numbers of molecular devices (~10^{23}), every one of which is structurally the same. However, several issues may arise in the syntheses and also in the interconnection of these devices to form large circuits. It is likely that a fraction of the devices will not be operational simply because of the statistical yields of the chemical syntheses used to make them. That is, while chemical syntheses yield operational devices that are all structurally the same, a feat that is not possible by conventional microfabrication methods [71], any series of chemical syntheses with less than one hundred percent yield will produce both operational and non-operational devices. Also, it may not be feasible to test all of them to select out the ones that are not operational. Further, most of the self-ordering chemical assembly processes that presently are being investigated would produce a large amount of randomness and uncertainty in the connectivity among large numbers of molecular device structures in a system.

One approach for addressing these challenges is to design an architecture that is inherently defect-tolerant. Even with many defects, the architecture would have the capability of operating as desired without physically repairing or removing defects incorporated into the system during the assembly process. Heath *et al.* recently discussed the demonstration of such a defect-tolerant computer architecture built from solid-state components and, for that system, it was discovered that the execution time for many algorithms was surprisingly fast, operating at 100 times faster than a high-end single-processor workstation for some of its configurations [72].

Due in part to the issues and challenges discussed above, it is likely that nanometer-scale solid-state memories will be realized fully before molecular electronic memories are. In fact, several types of nanoelectronic solid-state memory [24-27] have been proposed, analyzed, fabricated, and demonstrated in individual nanometer-scale memory cells or small aggregations of such cells. However, the problem of fabricating trillions of solid-state nanoelectronic memory cells uniformly and defect-free is still a large obstacle [71]. On the other hand,

the recent achievements in the synthesis of molecules by Tour and others demonstrate that molecular devices can be synthesized in very large numbers, as large as ~10^{23}, every one of which is of exactly the same structure and size [51, 20, 21]. These achievements in fabrication and synthesis strongly suggest that it will be possible to manufacture molecular-scale memory economically and in quantity.

V. SUMMARY AND CONCLUSIONS

A. A step toward a compatible ultra-dense electronic memory

This paper builds upon previous research in solid-state nanoelectronic memory and molecular electronics to present designs for molecular electronic digital memory cells. The recent rapid refinement of solid-state nanoelectronic devices [31] permitted the design and demonstration of the solid-state quantum-effect TSRAM, which combines the advantages of both microelectronic DRAM and SRAM. Similarly, recent exciting developments in the synthesis and demonstration of molecular electronic devices inspired the ME-TSRAM design that is detailed and discussed in this paper.

In describing this ME-TSRAM design, we have outlined an approach for the miniaturization of electronic digital memory circuitry down to the molecular scale, while preserving many of the features that are both familiar and advantageous in present-day micron-scale designs. The ME-TSRAM is structurally similar to a microelectronic DRAM, as is suggested by the similarities between the TSRAM cell circuit diagram, displayed in Figure 2(a), and the DRAM cell circuit diagram, displayed in Figure 4(b). Also, the ME-TSRAM is operationally similar to a microelectronic SRAM since it proposes to store bits without any periodic refresh (although, unlike SRAM, the ME-TSRAM must refresh a cell each time it is read. As detailed above, by preserving these features present in microelectronic designs, one is able to conceptualize a molecular electronic design that combines the advantages of both types of conventional memory.

Some other approaches to making nanometer-scale electronic memories [7, 24-27] also retain this structural and functional similarity to microelectronic memory. However, they do not achieve the same degree of miniaturization. On the other hand, most, if not all the proposed approaches that are comparable to the anticipated size and density of the ME-TSRAM cell are very different from present-day microelectronic memory in their structure and in their principles of operation [73-77].

Thus, with ME-TSRAM, one might be able to continue or exceed the Moore's Law trend [23], while retaining the well-tested system designs and architectures, as well as the design flexibility, that have helped make microelectronic memory such a successful technology and such a valuable commodity.

B. An essential step toward an important societal goal

At this stage of the miniaturization revolution, the development of molecular-scale electronic memory, such as ME-TSRAM, also appears to be a key step which must be taken to further the societal goals of continued technological and economic progress. The miniaturization of digital electronics, as governed by Moore's Law, has been at the root of the information technology revolution and the rapid, dramatic, long-lived economic and technological progress associated with it. Continuation of this prosperity, therefore, demands the continued miniaturization of digital electronics and, hence, the development of ultra-dense computer circuitry.

For a number of reasons, though, efforts to develop ultra-dense computer circuitry are leading, inexorably, toward molecular electronics and molecular electronic memories. Unlike micron-scale electronic devices and circuits, nanometer-scale electronic switching devices and ultra-dense circuitry that incorporate quantum effects must take advantage of them if they are to operate efficiently. To take advantage of quantum effects and still operate at room temperature, the essential structure of a device should measure considerably less than 100 nm. Further, to achieve the desired uniformity in the function of any two or more nanometer-scale, quantum-effect devices, quantum principles dictate that their dimensions must be the same within tolerances of approximately one atomic diameter [31]. However, this small size and degree of precision in the fabrication of solid-state devices and circuits is very difficult, if not impossible, to achieve economically using lithographic or other presently available methods.

Molecules, on the other hand, are "natural" nanometer-scale structures. They can be made very cheaply in enormous numbers (~10^{23}), and every molecule of a given type is the same size and structure down to the atomic scale and below (disregarding transient, controllable conformational variations) [30]. This means that individually conductive molecules have some very great

advantages over conventional solid-state structures for making large numbers of nanometer-scale electronic devices and extended ultra-dense circuitry integrated on the nanometer scale. In addition, it has been demonstrated recently that some molecules--notably polyphenylenes and carbon nanotubes--individually can carry surprisingly large currents of electrons [1].

Thus, the societally necessary effort to develop ultra-dense electronic computers leads, inexorably, to an effort to develop a computer made from conductive molecular wires and devices. This, in turn, requires the development of a molecular electronic memory, since most all architectures for electronic computers demand a memory unit as well as a processor. Moreover, even the processor almost always requires a considerable amount of fast, electronically addressable memory mixed in with its logic circuits.

Thus, the development of molecular electronic memory arguably is a key step on the critical path to further economic progress. More specifically, it would be best if the ultra-dense molecular electronic memory that is developed initially were to represent an evolutionary step forward, as does ME-TSRAM. Then, the memory might even be integrated in a simple way into existing microelectronic processor architectures. A design for molecular electronic memory that can meet these criteria would not only ensure long term technological progress, but also a more rapid, smooth, and economically advantageous transition to next-generation computers by way of "hybrid" microelectronic-molecular electronic circuitry.

This is the special niche that the authors envision for a molecular electronic memory cell like the one described in this paper. It is hoped that the ME-TSRAM design will help to probe the limits of miniaturization for a memory cell and also assist in making the necessary smooth transition from microelectronics to molecular electronics, while it paves the way for purely molecular electronic computers.

ABOUT THE AUTHORS

Greg Y. Tseng began his research on ultra-dense nanometer-scale electronic memories in 1997 as a member of the MITRE Nanosystems Group. Presently, he is a John Harvard Scholar at Harvard College and expects to receive his A.B. in Physics and Mathematics in June 2001. Greg also is performing research at Harvard University on carbon nanotube-based molecular electronics. He is a 1997 graduate of Thomas Jefferson High School for Science and Technology in Alexandria, Virginia, where he was a finalist in the 56th Westinghouse Science Talent Search for his research in fiber optic biochemical sensing.

Dr. James C. Ellenbogen is Principal Scientist in the Nanosystems Group at The MITRE Corporation and Principal Investigator of MITRE's Nanosystems Modeling and Nanoelectronic Computers Research Project. Dr. Ellenbogen received his Ph.D. in chemical physics from the University of Georgia in 1977. He is the author of a number of technical papers on the modeling, simulation, and testing of military systems, on the theory of command and control, and on diverse topics in computer science, physics, and chemistry. He taught at several universities before joining the MITRE Corporation in 1984. Since 1993 he has devoted his energies to furthering the science and technology for designing and developing electronic computers integrated on the nanometer scale. In that effort he has collaborated in the development of unique designs for nanoelectronic devices and co-authored several widely cited technical articles on nanoelectronics.

ACKNOWLEDGMENTS

The authors are grateful to other members of the MITRE Nanosystems Group, especially David Moore and J. Christopher Love, for their collaboration in the nanoelectronics research investigations which led up to and supported the one upon which this paper is based. Kevin Wegener of the Nanosystems Group also made invaluable contributions in his careful reading, editing, and suggestions for an earlier version of this manuscript. Prof. Jerry Iafrate of The University of Notre Dame offered us much kind assistance in the calculation and interpretation of molecular capacitances, and we thank him. Further, we thank Paul van der Wagt, Gary Frazier, Alan Seabaugh, and others from the Nanoelectronics Group at Raytheon-TI Research Laboratories for providing us with copies of their unpublished manuscripts about solid-state TSRAM. We are also grateful to Drs. William Warren and Bruce Gnade of the Defense Advanced Research Projects Agency for their encouragement of this line of investigation over the past year. We are much indebted, in addition, to many of our other colleagues at MITRE for their invaluable long-standing support of this research, notably David Lehman, Steven Huffman, Edward Palo, William Hutzler, Karen Pullen, and Kerry Butterfield. This research was funded by a grant from The MITRE Corporation.

REFERENCES

[1] J. C. Ellenbogen and J. C. Love, "Architectures for molecular electronic computers: 1. Logic structures and an adder built from molecular electronic diodes," No. MP 98W0000183, The MITRE Corporation, McLean, VA, July 1999.

[2] J. C. Ellenbogen, "Architectures for molecular electronic computers: 2. Logic structures using molecular electronic transistors," The MITRE Corporation, McLean, VA, Manuscript in preparation.

[3] A. C. Seabaugh *et al.*, "Silicon-based quantum MOS technology," *Proc. 1998 Government Microelectronics Conference*, Arlington, VA, pp. 377-380, 1998.

[4] J. P. A. van der Wagt, A. C. Seabaugh, and E. A. Beam III, "RTD/HFET low standby power SRAM gain cell," *Int. Electron Device Meet. Tech. Dig.*, pp. 425-428, 1996.

[5] J. P. A. van der Wagt, A. C. Seabaugh, and E. A. Beam III, "RTD/HFET Low Standby Power SRAM Gain Cell," *IEEE Electron Device Lett.*, vol. 19, pp. 7-9, 1998.

[6] J. P. A. van der Wagt *et al.*, "Tunneling-based static random access memory," *Proc. 1998 Government Microelectronics Conference*, Arlington, VA, pp. 238-241, 1998.

[7] J. P. A. van der Wagt, "Tunneling-based SRAM," *Proc. IEEE*, vol. 87, pp. 571-595, 1999.

[8] J. P. A. van der Wagt, "Memory Cell Having Negative Differential Resistance Devices," United States Patent No. 5,883,829, 16 March 1999.

[9] J. M. Tour, R. Wu, and J. S. Schumm, "Extended Orthogonally Fused Conducting Oligomers for Molecular Electronic Devices," *J. Am. Chem. Soc.*, vol. 113, pp. 7064-7066, 1991.

[10] J. M. Tour, "Chemical Synthesis of Molecular Electronic Devices," presented at 1997 DARPA ULTRA Review Conference, Santa Fe, NM, October 1997. This presentation discussed the synthesis of a molecular RTD, as well as the strategy for inserting acetylenic linkages between aromatic rings in polyphenylene-based molecular wires to reduce the steric interence between the hydrogen atoms bonded to adjacent aromatic phenyl groups in the molecular wire.

[11] J. M. Tour, "Conjugated Macromolecules of Precise Length and Constitution. Organic Synthesis for the Construction of Nanoarchitectures," *Chem. Rev.*, vol. 96, pp. 537-554, 1996.

[12] J. S. Schumm, D. L. Pearson, and J. M. Tour, "Iterative Divergent/Convergent Approach to Linear Conjugated Oligomers by Successive Doubling of the Molecular Length: A Rapid Route to a 128 Å-Long Potential Molecular Wire," *Angew. Chem. Int. Ed. Engl.*, vol. 33, pp. 1360-1363, 1994.

[13] L. Jones, J. S. Schumm, and J. M. Tour, "Rapid solution and solid phase syntheses of oligo (1,4-phenylene-ethynylene)s with thioester termini: Molecular scale wires with alligator clips. Derivation of iterative reaction efficiencies on a polymer support," *J. Organic Chem.*, vol. 62, pp. 1388-1410, 1997.

[14] L. A. Bumm *et al.*, "Are Single Molecular Wires Conducting?," *Science*, vol. 271, pp. 1705-1707, 1996.

[15] A. Dhirani *et al.*, "Self-assembled molecular rectifiers," *J. Chem. Phys.*, vol. 106, pp. 5249-5253, 1997.

[16] R. M. Metzger *et al.*, "Unimolecular Electrical Rectification in Hexadecylquinolinium Tricyanoquinodimethanide," *J. Am. Chem. Soc.*, vol. 119, pp. 10455-10466, 1997.

[17] L. Ottaviano *et al.*, "Rectifying behavior of silicon-phthalocyanine junctions investigated with scanning tunneling microscopy/spectroscopy," *J. Vac. Sci. Technol. A*, vol. 15, pp. 1014-1019, 1997.

[18] C. Zhou *et al.*, "Nanoscale metal/self-assembled monolayer/metal heterostructures," *Appl. Phys. Lett.*, vol. 71, pp. 611-613, 1997.

[19] M. A. Reed, "Molecular-Scale Electronics," *Proc. IEEE*, vol. 87, pp. 652-658, 1999.

[20] R. P. Andres *et al.*, "'Coulomb Staircase' at Room Temperature in a Self-Assembled Molecular Nanostructure," *Science*, vol. 272, pp. 1323-1325, 1996.

[21] R. P. Andres *et al.*, “The Design, Fabrication and Electronic Properties of Self-Assembled Molecular Nanostructures,” in *The Handbook of Nanostructured Materials and Nanotechnology*, H. S. Nalwa, Ed.: Academic Press, 1999.

[22] A. Aviram and M. A. Ratner, “Molecular Rectifiers,” *Chem. Phys. Lett.*, vol. 29, pp. 277-283, 1974.

[23] SIA, "The National Technology Roadmap for Semiconductors," Semiconductor Industry Association, Austin, TX, 1997.

[24] L. Guo *et al.*, “A Silicon Single-Electron Transistor Memory Operating at Room Temperature,” *Science*, vol. 275, pp. 649-651, 1997.

[25] S. Tiwari *et al.*, “A silicon nanocrystals-based memory,” *Appl. Phys. Lett.*, vol. 68, pp. 1377-1379, 1996.

[26] J. P. A. van der Wagt, G. Frazier, and H. Tang, “High Density Memory Based on Quantum Device Technology,” presented at The International Conference on Integrated Micro-Nanotechnology for Space Applications, Houston, TX, 1995.

[27] J. J. Welser *et al.*, “Room Temperature Operation of a Quantum-Dot Flash Memory,” *IEEE Electron Device Lett.*, vol. 18, pp. 278-280, 1997.

[28] M. A. Reed, “Electrical Properties of Molecular Devices,” presented at 1997 DARPA ULTRA Program Review Conference, Santa Fe, NM, 26-31 October 1997. This presentation discussed the experimental measurement of a molecular RTD.

[29] M. A. Reed, Private communication, October 1997.

[30] M. S. Montemerlo, J. C. Love, G. J. Opiteck, D. J. Goldhaber-Gordon and J. C. Ellenbogen, "Technologies and Designs for Electronic Nanocomputers," No. MTR 96W0000044, The MITRE Corporation, McLean, VA, July 1996.

[31] D. Goldhaber-Gordon, M. S. Montemerlo, J. C. Love, G. J. Opiteck and J. C. Ellenbogen, “Overview of Nanoelectronic Devices,” *Proc. IEEE*, vol. 85, pp. 521-540, 1997. See also references cited in the extensive bibliography in this work.

[32] G. Maracas *et al.*, “Interfacing Molecules to External Electronics,” presented at DARPA Molecular Electronics Workshop, Reston, VA, 3-4 February 1998. This presentation tabulated the results of recent experiments measuring the electrical properties of small molecules.

[33] D. C. Moore and J. C. Ellenbogen, "Architectures for molecular electronic computers: 4. Quantum calculations to determine electrical properties for molecular electronic rectifying diodes," The MITRE Corporation, McLean, VA, Manuscript in preparation.

[34] M. A. Ratner and J. Jortner, “Molecular Electronics: Some Directions,” in *Molecular Electronics*, M. Ratner J. Jortner, Ed. London, UK: Blackwell Science Ltd., 1997, pp. 5-72. See also references cited therein.

[35] M. Ratner, “Molecular Electronics: Interconnects, Gates, Energy Dissipation, and Multifunctionality,” presented at DARPA Molecular Electronics Workshop, Reston, VA, 3-4 February 1998. This presentation also tabulated the results of recent experiments measuring the electrical properties of small molecules.

[36] M. A. Reed *et al.*, “Conductance of a Molecular Junction,” *Science*, vol. 278, pp. 252-254, 1997.

[37] C. Zhou *et al.*, “Mesoscopic Phenomena Studied with Mechanically Controllable Break Junctions at Room Temperature,” in *Molecular Electronics*, J. Jortner and M. Ratner, Ed. London, UK: Blackwell Science Ltd., 1997, pp. 191-213.

[38] C. Dekker, “Carbon Nanotubes as Molecular Quantum Wires,” *Physics Today*, pp. 22-28, 1999.

[39] M. S. Dresselhaus, G. Dresselhaus and P. C. Eklund, *Science of Fullerenes and Carbon Nanotubes*. San Diego: Academic Press, 1996.

[40] T. W. Odom *et al.*, “Atomic Structure and Electronic Properties of Single-Walled Carbon Nanotubes,” *Nature*, vol. 391, pp. 62-64, 1998.

[41] M. S. Smith and J. C. Ellenbogen, "Architectures for Molecular Electronic

Computers: 5. Designs for Digital Logic Structures Constructed from Carbon Nanotubes," The MITRE Corporation, McLean, VA, Manuscript in preparation.

[42] S. J. Tans *et al.*, "Individual Single-Wall Carbon Nanotubes as Quantum Wires," *Nature*, vol. 386, pp. 474-477, 1997.

[43] S. J. Tans, Ph.D. thesis, Delft Technical University, 1998. See also the references cited therein, which give an excellent background on the fundamentals of the structure and electronic properties of carbon nanotubes or "buckytubes." This remarkable thesis is available in a version published by Delft University Press, Delft, The Netherlands, 1998.

[44] S. J. Tans, A. R. M. Verschueren, and C. Dekker, "Single nanotube-molecule transistor at room temperature," *Nature*, vol. 393, pp. 49-51, 1998.

[45] J. W. G. Wildöer *et al.*, "Electronic structure of atomically resolved carbon nanotubes," *Nature*, vol. 391, pp. 59-62, 1998.

[46] B. I. Yakobson and R. E. Smalley, "Fullerene Nanotubes: C(1,000,000) and Beyond," *American Scientist*, vol. 85, pp. 324-337, 1997. See also references therein.

[47] S. Datta *et al.*, "Current-Voltage Characteristics of Self-Assembled Monolayers by Scanning-Tunneling Microscopy," *Phys. Rev. Lett.*, vol. 79, pp. 2530-2533, 1997. This important theory paper points out that the actual conductance of molecular wires may be much higher than the measured conductance in some experiments.

[48] V. Mujica, M. Kemp, and M. A. Ratner, "Electron Conduction in Molecular Wires. I. A Scattering Formalism," *J. Chem. Phys.*, vol. 101, pp. 6849-6855, 1994.

[49] V. Mujica, M. Kemp, and M. A. Ratner, "Electron Conduction in Molecular Wires. II. Application to Scanning Tunneling Microscopy," *J. Chem. Phys.*, vol. 101, pp. 6856-6864, 1994.

[50] V. Mujica *et al.*, "Current-Voltage Characteristics of Molecular Wires: Eigenvalue Staircase, Coulomb Blockade, and Rectification," *J. Chem. Phys.*, vol. 104, pp. 7296-7305, 1996.

[51] J. M. Tour, M. Kozaki, and J. M. Seminario, "Molecular Scale Electronics: A Synthetic/Computational Approach to Digital Computing," *J. Am. Chem. Soc.*, vol. 120, pp. 8486-8493, 1998.

[52] B. Brar *et al.*, "Resonant Tunneling Technology for Ultra-High-Speed Circuits," *Proc. 1998 Government Microelectronics Conference*, Arlington, VA, pp. 222-225, 1998.

[53] R. H. Mathews *et al.*, "Resonant-Tunneling-Diode Digital Filters," *Proc. 1998 Government Microelectronics Conference*, Arlington, VA, pp. 373-376, 1998.

[54] P. Mazumder and K. Chakraborty, *Testing and Testable Design of High-Density Random-Access Memories*. Boston: Kluwer Academic Publishers, 1996.

[55] B. Prince, *High Performance Memories: New Architecture DRAMs and SRAMs--Evolution and Function*. New York: John Wiley & Sons, 1996.

[56] M. M. Cirovic, *Handbook of Semiconductor Memories*. Reston, VA: Reston Publishing Company, 1981.

[57] F. F. Driscoll, *Microprocessor-Microcomputer Technology*. New York: Van Nostrand Reinhol Company, 1983.

[58] M. A. Reed, "Progress in Molecular-Scale Devices and Circuits," presented at 57th Annual IEEE Device Research Conference, Santa Barbara, CA, 28-30 June 1999. This presentation contained information about an intramolecularly doped polyphenylene-based molecular RTD which exhibited an extremely large switching transition, a 1000:1 peak-to-valley current ratio, with an approximately 1 nanoamp peak current at 60 degrees Kelvin, under an approximately 2 volt bias. The molecular structure was synthesized by Prof. James Tour of Rice University and tested by Prof. Reed and his collaborators at Yale University. We thank Profs. Reed and Tour for sharing these recent results with us.

[59] D. F. Bocian, "Multiporphyrin memory systems," presented at DARPA Moletronics Principal Investigator's Meeting, Ashburn, VA, 8-9 July 1999.

[60] L. R. Milgrom, *The Colours of Life: An Introduction to the Chemistry of Porphyrins and Related Compounds*. Oxford: Oxford University Press, 1997.

[61] E. Alder et al. "The evolution of IBM CMOS DRAM technology," IBM J. Res. Dev., Vol. 39, 1995, p. 167. This paper can be found on the Internet at the URL: http://www.research.ibm.com/journal/rd/adler/adler.html

[62] G. J. Iafrate, K. Hess, J. B. Krieger, and M. Macucci, "Capacitive nature of atomic-sized structures," *Phys. Rev. B*, vol. 52, pp. 10737-10739, 1995.

[63] M. Macucci, K. Hess, and G. J. Iafrate, "Electronic energy spectrum and the concept of capacitance in quantum dots," *Phy. Rev. B.*, vol. 48, pp. 17354-17363, 1993.

[64] M. Macucci, K. Hess, and G. J. Iafrate, "Simulation of electronic properties and capacitance of quantum dots," *J. Appl. Phys.*, vol. 77, pp. 3267-3276, 1995.

[65] G. J. Iafrate, Private communication, June-July 1999

[66] Spartan version 5.0, Wavefunction, Inc., 18401 Von Karman Avenue, Suite 370, Irvine, CA 92612, U.S.A.

[67] Gaussian 98, Gaussian, Inc., Carnegie Office Park, Building 6, Pittsburgh, PA 15106, U.S.A.

[68] M. A. Ratner *et al.*, "Molecular Wires: Charge Transport, Mechanisms, and Control," in *Molecular Electronics: Science and Technology*, vol. 852, *Ann. N.Y. Acad. Sci.*, A. Aviram and M. Ratner, Eds.: New York Academy of Sciences, 1998, pp. 22-37.

[69] J. C. Love and G. Y. Tseng, The MITRE Corporation, McLean, VA. Work in progress.

[70] A. Bezyradin *et al.*, "Multiprobe transport experiments on individual single-wall carbon nanotubes," *Phys. Rev. Lett.*, vol. 80, pp. 4036-4039, 1998.

[71] R. F. Service, "Making Single Electrons Compute," *Science*, vol. 275, pp. 303-304, 1997.

[72] J. R. Heath *et al.*, "A Defect-Tolerant Computer Architecture: Opportunities for Nanotechnology," *Science*, vol. 280, pp. 1716-1721, 1998.

[73] C. M. Lieber, "Towards a Nanotube-Based Computer," presented at DARPA Moletronics Principal Investigator's Meeting, Ashburn, VA, 8-9 July 1999.

[74] D. Tomanek, "Use of Self-Assembled Nanotubes as Memory and Logic Devices," presented at DARPA Moletronics Principal Investigator's Meeting, Ashburn, VA, 8-9 July 1999.

[75] D. Berzon and T. Fountain, "Computer Memory Structures using QCAs," No. 98/1, Image Processing Group, Department of Physics and Astronomy, University College-London, London, UK, 1998.

[76] M. Lieberman, "Molecular Electronics Based on Quantum Dot Cellular Automata," presented at DARPA Moletronics Principal Investigator's Meeting, Ashburn, VA, 8-9 July 1999. Prof. Lieberman's work involves the miniaturization of quantum dot cells to the molecular scale. In order to implement the memory strategy proposed by Fountain and his collaborators [73], and to achieve reliable high temperature operation, one would probably need molecular-scale quantum dot cells of the type being developed by Prof. Lieberman and her collaborators

[77] C. P. Collier *et al.*, "Electronically Configurable Molecular-Based Logic Gates," *Science*, vol. 285, pp. 391-394, 1999.