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# On the Scaling of Electronic Charge-Storing Memory Down to the Size of Molecules

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McLean, Virginia



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## **SUMMARY**

This investigation quantitatively explores the possibility of shrinking electronic, charge-storing, random access memory to the molecular-scale. The results suggest that quantum effects may hinder the operation of electronic memory on such small scales, but this effect is not pronounced enough to prevent its functioning. Thus, it should be possible to build and operate such memory at densities 10,000 to 100,000 times greater than present-day memory.



## ABSTRACT

This paper presents an analysis of the performance impact of scaling present-day micrometer-scale, charge-storing random-access memory (RAM) down to the scale of proposed molecular electronic memory. As a part of this analysis, the likely performance is determined for arrays of molecular-scale memory 10,000 to 100,000 times denser than present-day memory. A combination of classical and quantum mechanical methods are employed to calculate the properties of nanometer-scale devices and memory systems. These calculations suggest that quantum mechanics and other small-scale effects should decrease the capacitance and increase the resistance of molecular-scale circuit components. However, these trends are not pronounced enough to prevent the operation of charge-storing memory on that scale. Some forms of molecular-scale memory built entirely from existing nanometer-scale devices should be able to function nearly as fast as present-day memory.



## INTRODUCTION

This paper presents an analysis of the performance impact of scaling present-day micrometer-scale, charge-storing memory down to the nanometer-scale of proposed molecular electronic memory. This question is important both scientifically and economically. This is because such molecular memory could store data at least 20,000 times more densely than present-day memory and also because recent advances in nanoelectronics are bringing the manufacture of molecular electronic systems closer to realization.

In the past several years, there have been numerous demonstrations of molecular wires and two-terminal switches [2]; very recently three-terminal molecular-scale transistors and logic gates also have been demonstrated [3-7]. The discovery of the properties of these devices sheds light on the question of how the properties of individual electronic components change as they are shrunk or “scaled” from the micrometer to the nanometer domain. It also raises the question of how the operational constraints and the likely performance of entire electronic systems will change when they are miniaturized to the nanometer scale.

Memory would seem to be an excellent candidate for such an investigation of the scaling of circuits and systems because of its invariant, regular structure, which facilitates analysis, as well as fabrication. However, the analysis does present special challenges, at least because it is necessary to account for the quantum mechanical effects in the structures and dynamics of future nanometer-scale memory cells and array components.

To meet these challenges, in this investigation the quantitative analysis of the scaling of arrays of charge-storing memory cells is performed in two parts. The first is an analysis of molecular-scale electronic memory. In this part, primarily classical circuit laws are used to derive requirements for the properties of components of molecular-scale memory arrays. Simple expressions and differential equations are given that describe the performance of such memory. Quantum mechanical analysis is used to calculate the properties of actual nanometer-scale devices, which are used with the above-mentioned requirements and equations to determine the likely performance of molecular-scale memory composed of such devices.

The second part of the analysis is a purely classical extrapolation of the electrical behavior of present-day microelectronic memory down to the molecular scale. In this part, it is assumed that the classical laws that govern the behavior of memory on the micrometer scale do not break down on the nanometer scale because of quantum mechanics and other small-scale effects. With this assumption, the properties of nanometer-scale electronic devices are calculated and the likely performance of memory composed of such devices is determined.

The results of this two-part analysis are summarized in Table 1. In the Discussion section following the analysis, a comparison is made of the results from the two parts of the analysis. This comparison suggests that in the nanometer domain resistances will be larger and capacitances smaller than might be expected from a purely classical extrapolation. Note in the last row of Table 1, the device resistance for the molecular memory array is greater than for the extrapolation presented in the row above. In the analogous comparison involving the storage node capacitances, the capacitance of the molecular memory clearly is much smaller than the extrapolated value presented above it. However, the results also suggest that these effects are not necessarily large and should not prevent the operation of molecular-scale memory. The molecular-scale memory described in this paper will likely have a longer read access time than conventional memory, and will thus operate more slowly. However, it still will be likely to function effectively, attaining bit densities as large as 2.5 terabits/cm<sup>2</sup>, which is 10,000 to 100,000 times denser than present-day memory.

**Table 1. Summary of Results Predicting the Performance of Charge-Storing Memory**

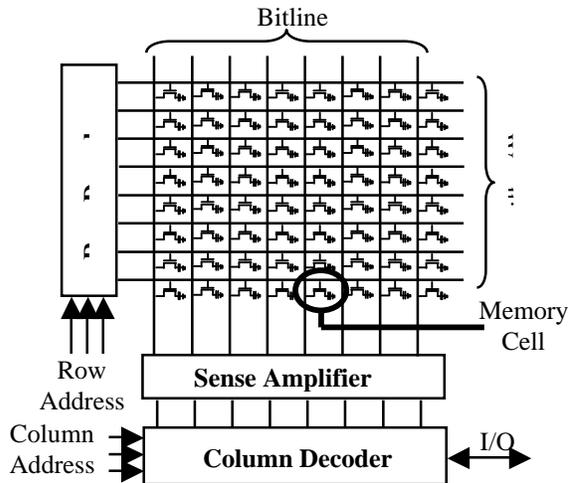
		Cell Size (nm <sup>2</sup> )	Device Resistance (Ω)	Capacitance of Storage Node (F)	Capacitance of Bitline (F)	Access Time (s)
Micron Scale	Micrometer-Scale Conventional SRAM	4,600,000	18,000	N/A	1.6 × 10 <sup>-13</sup>	7.2 × 10 <sup>-11</sup>
	Micrometer-Scale Conventional DRAM	260,000	18,000	2.5 × 10 <sup>-14</sup>	1.1 × 10 <sup>-13</sup>	1.1 × 10 <sup>-9</sup>
Nanometer Scale	SRAM Extrapolated to Molecular Scale	530	1.7 × 10 <sup>6</sup>	N/A	1.3 × 10 <sup>-15</sup>	1.8 × 10 <sup>-11</sup>
	DRAM Extrapolated to Molecular Scale	30	1.7 × 10 <sup>6</sup>	2.5 × 10 <sup>-14</sup>	1.0 × 10 <sup>-15</sup>	4.9 × 10 <sup>-9</sup>
	Molecular Memory Array	40	3.0 × 10 <sup>10</sup>	4 × 10 <sup>-20</sup>	1.3 × 10 <sup>-16</sup>	1.1 × 10 <sup>-7</sup>

## BACKGROUND

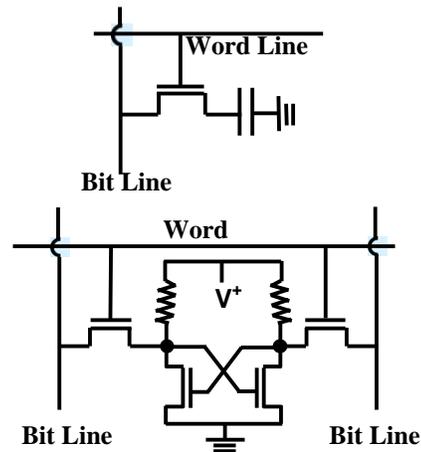
This section reviews a few basic concepts and principles of microelectronics and nanoelectronics that are essential for the scaling analysis that follows. Specifically, a summary is given of the design and operation of microelectronic memory and for a type of quantum-effect nanoelectronics memory. A detailed explanation is given of the role of capacitance in stored-charge memory.

Although electronic computers use many types of information storage, this paper will use the term “memory” only to refer to fast, electronically addressable random access memory (RAM). The fundamental unit of RAM is the memory cell. Each cell represents a bit of information – a “1” or a “0” – by the presence or absence of charge in its circuitry. Cells are arranged in two-dimensional arrays, as shown in Figure 1. Each is accessed by a crossbar of horizontal and vertical wires called wordlines and bitlines. Arrays have accompanying circuitry that take memory addresses and read the data out of the appropriate cells. An entire memory chip contains many arrays and the circuitry used to access them [8].

**Figure 1. A schematic of a memory array.**



**Figure 2. Schematics of (a) a Dynamic RAM cell (DRAM) and (b) a Static RAM cell (SRAM)**

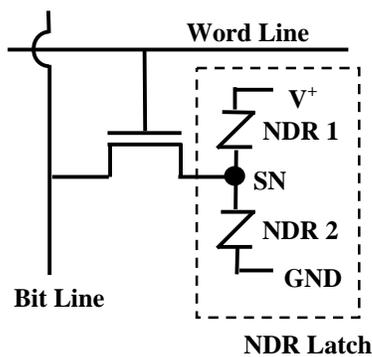


RAM is divided into two broad categories, Dynamic RAM (DRAM) and Static RAM (SRAM), as illustrated schematically in Figure 2. DRAM stores information in a single capacitor connected to the rest of the computer by a transistor. This is shown in Figure 2(a). The charge in a DRAM cell is transferred to the bitline during a read operation. This charge will dissipate over time, so DRAM cells constantly need to have their values restored, an operation called “refreshing.” SRAM stores information in a number of logic

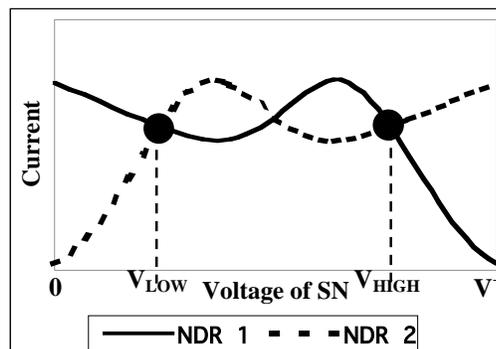
gates that hold a “1” or a “0” in the cell. A schematic of a typical SRAM cell is shown in Figure 2(b). The SRAM logic gate circuits are larger than the single capacitor in a DRAM cell, but they retain their value during a read operation and never need to be refreshed. SRAM is generally faster than DRAM and uses less power because it requires no refresh operation. However, DRAM is usually used in commercial systems because it is much smaller than SRAM. Each DRAM cell requires only a single transistor whereas an SRAM cell typically requires six [8].

A third and more recently developed type of memory stores information through a latch formed from negative differential resistance (NDR) switches placed in series. A schematic of such a memory appears in Figure 3. When two NDR switches are placed in series to form an NDR latch, the resulting circuit is bistable, as is shown in Figure 4. In NDR-based RAM, the lower voltage stable state, where  $V_{SN} = V_{LOW}$ , represents a “0” and the higher voltage state, where  $V_{SN} = V_{HIGH}$ , represents a “1”.

**Figure 3. A schematic of RAM employing an NDR latch.**



**Figure 4. Bistable current vs. voltage behavior for an NDR latch**



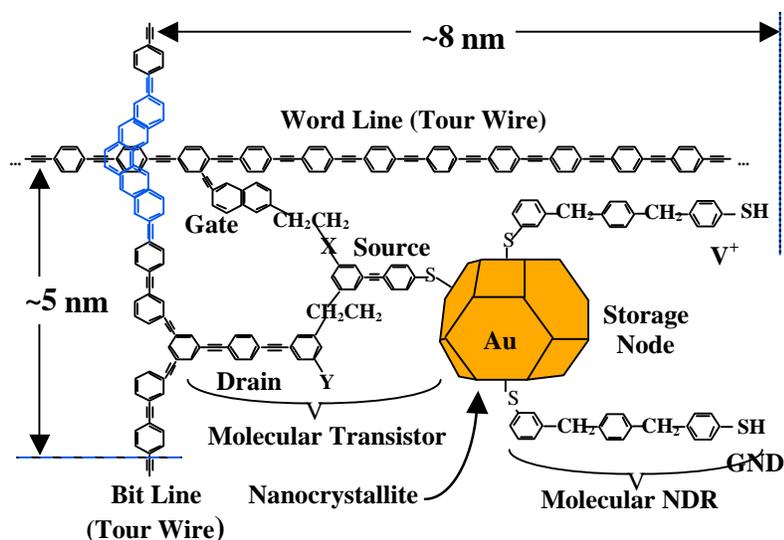
NDR-based memory can be designed to operate like dynamic or static RAM. In 1992, researchers at Fujitsu Laboratories developed and demonstrated Single-Transistor SRAM, a static memory cell using an NDR latch [9]. In 1995, researchers at Raytheon-TI developed and tested Tunneling-based Static RAM (TSRAM), a memory cell whose data was lost during read operations, like in DRAM, but which did not require periodic refresh operations because its data was maintained by an NDR latch [10,11].

Historically, DRAM has been recognized as the technology driver for the miniaturization of the component devices of computers [12]. The rapid and economically vital growth of computing power over the past forty years has been enabled by this miniaturization trend. However, this trend is nearing its

physical limit. It is generally believed that in ten to fifteen years, the computer industry will reach the point where transistors and other fundamental computer components cannot be shrunk any further because the quantum effects that operate on that scale will prevent their functioning. Nanoelectronics is an approach for continuing this miniaturization by building computers from nanometer-scale components that take advantage of quantum mechanics and other small-scale effects. Molecular electronics pursues this goal by constructing nanometer-scale wires and switches not from conventional silicon and metal, but from individual conductive molecules [13].

A number of nanoelectronic memory designs have been proposed and some nanometer-scale memory cells have been demonstrated [1,14-17,35]. This paper considers only those nanometer-scale memories that represent information with stored charge, as microelectronic memory does. One such memory is molecular electronic TSRAM (ME-TSRAM), designed at the MITRE Corporation in 1997 by Tseng and Ellenbogen [1]. An ME-TSRAM cell is shown in Figure 5. It is a molecular implementation of the TSRAM described and diagrammed previously above. The wordlines and bitlines are molecular wires of the same type fabricated by Tour *et al.* and demonstrated by Weiss *et al.* and by Zhou. The resonant-tunneling diodes are Tour wires with inserted aliphatic CH<sub>2</sub> groups fabricated by Tour *et al.* and demonstrated by Reed *et al.* A resonant-tunneling transistor proposed by Ellenbogen is employed as a transistor. A gold nanocrystallite demonstrated by Reifenberger *et al.* or a porphyrinic molecule is

**Figure 5. A diagram of Tseng and Ellenbogen's Molecular Electronic TSRAM cell [1]**



employed as molecular capacitor. The properties and development of these devices is described in greater detail elsewhere [1,2].

Central to the analysis of a charge-storing memory such as ME-TSRAM is the concept of capacitance, which is a measure of how easy it is to store charge on a device. Capacitance is defined as the constant of proportionality  $C$  in the equation

$$Q = CV, \quad (1)$$

where  $Q$  is the charge on a plate of a capacitor and  $V$  is the voltage difference between the two plates of the capacitor. Although capacitance is defined in terms of capacitors composed of two separated conductors, any electronic device, such as a wire or a gold cluster, can be considered a capacitor and thus has a capacitance. The device is one “plate” and the other “plate” is ground or “at infinity.” Putting a charge onto a device produces a voltage that repels the addition of further charge in accordance with Equation (1). The larger the capacitance of a device, the more charge can be held on that device with some fixed voltage [18]. In classical electrostatics, the capacitance of a structure is independent of the charge added, being a function only of the structure’s geometry and dielectric permittivity.

The issue of capacitance becomes more complicated at the molecular level. Nonetheless, the concept of capacitance is still valid as a means of describing how difficult it is to add charge to a molecular-scale structure. In a 1995 paper, Iafrete *et al.* derived a formula for the capacitance,  $C(N)$ , of a closed-shell  $N$ -electron molecular-scale system [19]:

$$C(N) = \frac{e^2}{IP(N) - EA(N)}, \quad (2)$$

where  $IP(N)$  is the ionization potential of the  $N$ -electron system,  $EA(N)$  is the electron affinity of the system, and  $e$  is the fundamental unit of charge. Note that the molecular capacitance,  $C(N)$ , is a function of the number of electrons in the system rather than being independent of the system’s charge.

## APPROACH

The remainder of this paper will apply the quantum capacitance concept defined in the previous section to the scaling analysis of the charge-storing memory designs that also are discussed in the

Background. As is explained in the Introduction, the two parts of the analysis are: (A) a calculation of the performance of molecular-scale memory and (B) a classical extrapolation of the electrical properties of microelectronic memory down to the molecular scale. The calculated properties of molecular-scale memory will be compared with the extrapolated properties in the Discussion section following the analysis.

## ANALYSIS & RESULTS

### ANALYSIS OF MOLECULAR-SCALE MEMORY

In this section, first, requirements are derived for the components of molecular-scale memory arrays, as are expressions for the performance of such memory as a function of its component's properties. The properties of existing nanometer-scale wires, switches, and capacitive storage nodes are then determined either from reported measurements or from quantum calculations. Table 2 shows these device properties and the calculated likely performance of memory arrays composed of such devices. Note that the Dynamic RAM and the Dynamic NDR-RAM are predicted not to function. The Hybrid and Static NDR-RAM are predicted to have access times of 110 nanoseconds, which is approximately two orders of magnitude slower than conventional RAM. The molecular SRAM may have an access time as small as 20 picoseconds, considerably faster than conventional RAM.

**Table 2. Predicted Performance of Molecular-Scale Memory Composed of Existing Nanometer-Scale Devices**

$R_{BL}$  is the resistance of the path electrons take from the storage node onto the bitline.  $R_{CELL}$  is the resistance of the circuitry in each memory cell that brings charge from  $V^+$  onto the storage node, if such circuitry exists. More detailed information on what  $R_{BL}$  and  $R_{CELL}$  correspond to in each type of memory can be found later in this section. The uncertainty in the values of  $R_{BL}$  and  $R_{CELL}$  is also discussed below.

Molecular-Scale Memory	Cell Size (nm <sup>2</sup> )	Capacitance of Storage Node (F)	Capacitance of Bitline (F)	$R_{BL}$ ( $\Omega$ )	$R_{CELL}$ ( $\Omega$ )	Access Time (s)
DRAM	30	$4.0 \times 10^{-20}$	$1.3 \times 10^{-16}$	$\sim 10^7$	N/A	not functional
Dynamic NDR-RAM	40	$4.0 \times 10^{-20}$	$1.3 \times 10^{-16}$	$\sim 10^7$	$3.3 \times 10^9$	not functional
Hybrid NDR-RAM	40	$4.0 \times 10^{-20}$	$1.3 \times 10^{-16}$	$3.0 \times 10^{10}$	$3.3 \times 10^9$	$1.1 \times 10^{-7}$
Static NDR-RAM	40	N/A	$1.3 \times 10^{-16}$	$3.2 \times 10^{10}$	$3.3 \times 10^9$	$1.1 \times 10^{-7}$
SRAM	160	N/A	$2.6 \times 10^{-16}$	$\sim 10^7$	$\sim 10^7$	$2.2 \times 10^{-11}$

**Requirements for Dynamic RAM.** The primary requirement for DRAM is that each cell stores sufficient charge in its storage node (SN) to produce a readable voltage on the bitline (BL) during a read operation. A schematic of DRAM appears in Figure 6 on the next page. Before charging the wordline and

switching the transistor to connect the storage node and the bitline, the total charge on both is the sum of the charges residing on each. This can be stated in accordance with Equation (1):

$$Q = V_{SN} C_{SN} + V_{BL} C_{BL} . \quad (3)$$

When the two are connected, the system will reach an equilibrium in which this charge is shared between both components such that the voltage of each will be equal:

$$V = \frac{Q}{C_{SN} + C_{BL}} = \frac{V_{SN} C_{SN} + V_{BL} C_{BL}}{C_{SN} + C_{BL}} . \quad (4)$$

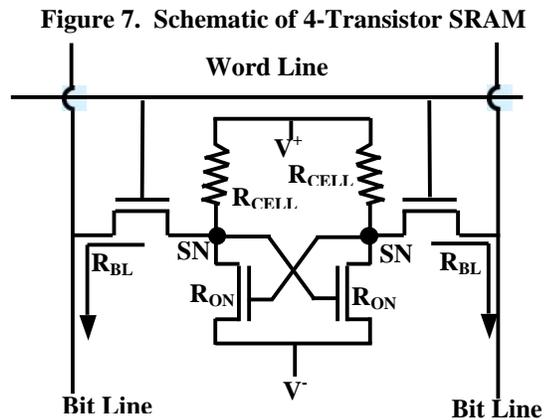
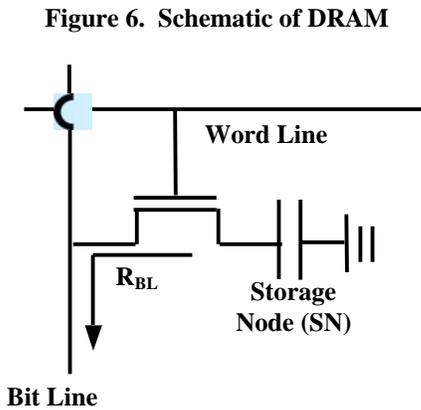
In coming to equilibrium, the voltage increase produced on the bitline is:

$$\Delta V = V - V_{BL} = \frac{V_{SN} C_{SN} + V_{BL} C_{BL}}{C_{SN} + C_{BL}} - V_{BL} = (V_{SN} - V_{BL}) \frac{1}{1 + C_{BL}/C_{SN}} . \quad (5)$$

The “transfer ratio”  $C_{SN}/C_{BL}$  of the capacitance of the storage node to that of the bitline must be large enough so that  $\Delta V$  is above the thermal noise threshold of 0.025 eV [1]. The amount of time it takes for the change in potential  $\Delta V$  to be produced on the bitline, which is an indicator of the speed of DRAM, is approximately:

$$\tau = 3RC , \quad (6)$$

where  $R$  and  $C$  are the combined capacitance and resistance of the bitline and storage node [1,8].



The second requirement on DRAM is that the storage node capacitance be large enough for the cell to have sufficient bit retention time and soft error immunity. Although DRAM cells are periodically refreshed, if a cell does not store enough charge, it’s value will have leaked out before it can be restored by

the refresh operation. Stray cosmic radiation or alpha particles from decaying isotopes in DRAM packaging can alter the amount of charge on a storage node, inducing a soft error if a memory cell does not have enough capacitance to maintain its value through such a change. The International Technology Roadmap for Semiconductors (ITRS) lists the minimum storage node capacitance for DRAM as approximately 25 fF to overcome these error-producing processes [12].

**Requirements for Static RAM.** In determining the requirements for SRAM, 4-transistor SRAM, pictured in Figure 7 on the previous page, is considered because the more commonly used 6-transistor SRAM requires both n-channel and p-channel transistors, whereas 4-transistor SRAM requires only n-channel transistors, which have been demonstrated at the molecular scale. The resistances and voltages in an SRAM cell must be chosen carefully so that the memory behaves correctly. The resistances  $R_{CELL}$ , the resistances  $R_{ON}$  for the transistors, and the voltages  $V^+$  and  $V$  must be selected so that  $V_{SN}$  is at a voltage of 0 or less when the transistor connecting it to  $V$  is on. During a read operation, the bitline connected to the storage node at 0 or less voltage will have no voltage increase. The bitline connected to the other storage node, which will be at voltage  $V^+$ , will slowly charge up to  $V^+$ . However, the speed of the read operation is dependent only on the time it takes for the bitline to experience a small voltage increase of  $\Delta V$ . As long as  $C_{SN} \ll C_{BL}$ , this time will be approximately:

$$\tau = C_{BL} \Delta V / I, \quad (7)$$

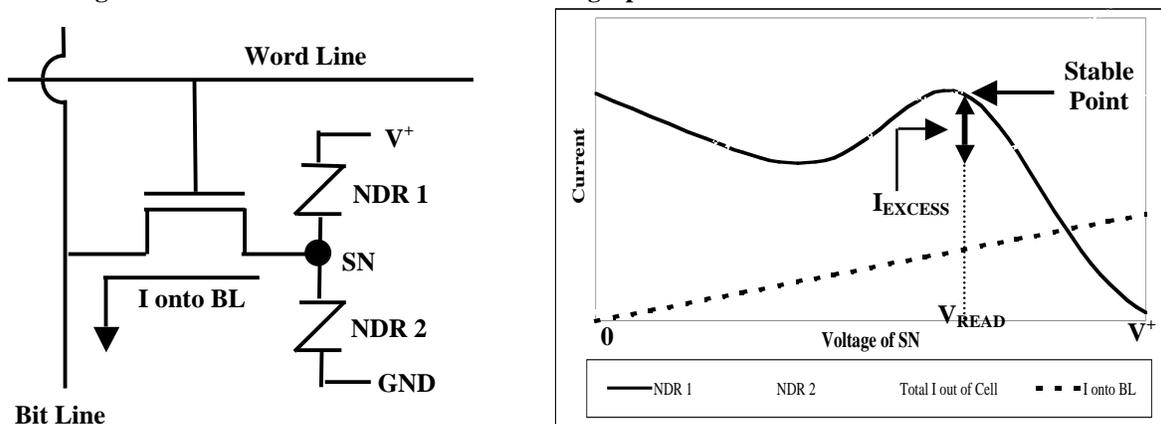
where  $I$  is the current from the storage node to the bitline during a read operation.

**Requirements for NDR-based RAM.** NDR-based RAM can operate like Dynamic RAM, Static RAM, or a hybrid of the two, and each mode of operation has a different set of requirements. NDR-based RAM operates “dynamically” when the charge put on the bitline during a read operation comes almost entirely from the storage node in the memory cell. This occurs only when the currents through the NDR-devices that form the memory cell’s NDR latch are so small that they can be ignored during a read operation. The read operation then consists entirely of charge sharing and destroys the value in the cell, like a read operation in a DRAM cell. Therefore, the same requirement applies that the transfer ratio  $C_{SN} / C_{BL}$  be large enough so that a readable voltage is produced on the bitline. For NDR-based RAM, the

requirement that the memory be immune to soft errors also still applies, but the requirement that it be able to retain data at least as long the time between refresh operations no longer applies because the NDR latch prevents leakage currents from destroying the stored value. The time required to perform a read operation is the time required for the charge sharing between the bitline and storage node, which is approximately  $3RC$ , as was discussed in connection with Equation (6).

NDR-based memory operates like static RAM when the charge placed on the bitline comes almost entirely from  $V^+$  through the NDR devices. The capacitance of the storage node no longer matters; the read operation is dependent instead on the NDR latch settling into a state where excess current is flowing onto the bitline, as in Figure 8. The read operation, like a read operation in SRAM, takes time  $C_{BL}\Delta V/I$  where  $I$  is the excess current from the latch onto the bitline.

**Figure 8. Schematic of NDR-based RAM and graph of currents in static NDR-based RAM**



Still a third type of read operation is possible for NDR-based RAM, a read operation in which the charge on the bitline comes partially from the storage node and partially from the power source  $V^+$  through the NDR devices. In this read operation, the storage node voltage decreases from  $V_{HIGH}$  to  $V_{LOW}$  as its charge is moved to the bitline, as in a dynamic read. However, the current through the NDR devices is large enough so that they add a significant amount of charge to the bitline as well. The only requirement on the memory is that the combined charge shared from the storage node and put on the bitline from  $V^+$  through an NDR device is measurable on the bitline. Intuitively, it can be seen that this results in requirements upon both the transfer ratio  $C_{SN}/C_{BL}$  and upon the current from the NDR latch onto the

bitline that are less stringent than for either the dynamic or the static read operations. This situation cannot be analytically modeled easily. Instead, it requires numerical integration of the differential equations that describe the motion of charge from  $V^+$  to the storage node, from the storage node to ground, and from the storage node to the bitline. These equations are:

$$\frac{dQ_{SN}}{dt} = f_{NDR}(V^+ - Q_{SN}/C_{SN}) - f_{NDR}(Q_{SN}/C_{SN}) - \frac{Q_{SN}/C_{SN} - Q_{BL}/C_{BL}}{R_{BL}} \quad (8)$$

and

$$\frac{dQ_{BL}}{dt} = \frac{Q_{BL}/C_{BL}}{R_{BL}}. \quad (9)$$

Above,  $Q_{SN}$ ,  $Q_{BL}$ ,  $C_{SN}$ , and  $C_{BL}$  are the charges and capacitances of the storage node and bitline, and  $f_{NDR}(V)$  is the current through the memory's NDR device when it is biased at  $V$  volts.  $R_{BL}$  is the combined resistance of the bitline and transistor. The first two terms in Equation (8) describe the current into and out of the storage node through the two NDR devices. The third term in Equation (8), which is the negative of the first term in Equation (9), describes the current between the storage node and the bitline. Equation (9) assumes that the circuitry used to sense the voltage on the bitline draws no current; another term easily could be added to incorporate such an effect. To use these equations to determine the time for a read operation,  $Q_{SN}$  initially is set to  $V_{HIGH}C_{SN}$  and  $Q_{BL}$  is set to  $V_{LOW}C_{BL}$ . When  $Q_{BL}$  reaches  $(V_{LOW} + \Delta V)C_{BL}$  and  $Q_{SN}$  drops to below  $(V_{HIGH} + V_{LOW})C_{SN}/2$ , the read operation is complete.

**Performance of Molecular-Scale DRAM and Dynamic NDR-Based RAM.** In order to assess whether molecular DRAM or molecular NDR-based RAM can operate effectively, the capacitances of the RAM's storage node and bitline must be determined. Of the nanometer-scale capacitive storage nodes proposed by Tseng and Ellenbogen [1], a gold nanocluster has the highest capacitance. This capacitance of  $4 \times 10^{-20}$  F was measured experimentally by P. Andres *et al* [20]. Of the many proposed nanometer-scale wires, Tour wires are the smallest, consisting only of a chain of benzene rings. Thus, they are likely to have the smallest capacitance of any proposed molecular wire. The capacitance of a Tour wire bitline extending the entire 5 nanometer length of one molecular memory cell is easily calculated as  $1.3 \times 10^{-19}$  using

Iafrate's formula [21]. However, bitlines in memory arrays extend the length of 512 or 1024. It is not computationally feasible to calculate the ionization potential and electron affinity of a Tour wire that is microns in length, so Iafrate's formula cannot be used directly to compute the capacitance of the bitline in a molecular memory array. Intuitively, it is clear that the capacitance of a molecular-scale structure should increase in some way as its size is increased. To simplify the analysis, it is assumed that the capacitance of a Tour wire increases in proportion to its length. The validity of this assumption presently is being investigated [32]. Therefore, the capacitance of a full-length Tour wire bitline should be approximately 1000 times that of a 5-nanometer Tour wire, or on the order of  $10^{-16}$  F. This yields a transfer ratio of less than 0.001. The minimum  $C_{SN}/C_{BL}$  ratio for a readable voltage increase to be produced on the bitline is approximately 0.1 [1], so the molecular DRAM and dynamic molecular NDR-based RAM under consideration probably would not function.

**Performance of Molecular-Scale Static NDR-Based RAM.** In calculating the properties of molecular static NDR-based RAM, this investigation considers memory built along the lines of the ME-TSRAM described in the Background. Tour-wire bitlines and wordlines are used, as is Ellenbogen's resonant tunneling transistor, but the resonant tunneling diodes are replaced with the NDR molecular switch developed and demonstrated by Chen *et al.* in 2000 [23], because they exhibit much higher conductance. When a latch incorporating these molecular switches is biased at 2.4 V, stable voltages exist at  $V_{LOW} = 0.744$  V and  $V_{HIGH} = 1.655$  V. If a bitline and transistor having a combined resistance of approximately  $3.2 \times 10^{10} \Omega$  is attached to the storage node in the latch, it results in an excess current onto the bitline of approximately 30 pA. From Equation (7), for that current to produce a voltage of 0.025 V during a read operation with a bitline capacitance of  $1.3 \times 10^{-16}$  F would take approximately 110 nanoseconds.

**Performance of Molecular-Scale Hybrid NDR-Based RAM.** The performance of molecular NDR-based RAM that is a hybrid of DRAM and SRAM is calculated Equations (8) and (9). With a bitline capacitance of  $1.3 \times 10^{-16}$  F, a storage node capacitance of  $4 \times 10^{-20}$  F, Chen *et al.*'s NDR-devices biased as in

the static NDR-based RAM, and a resistance  $R_{BL} \cong 3 \times 10^{10} \Omega$  for the bitline and transistor, a destructive read operation also takes approximately 110 nanoseconds.

**Performance of Molecular-Scale Static RAM.** Only a rough estimate can be made of the performance of molecular 4-Transistor SRAM. The resistances of short segments of Tour wires have been measured to be on the order of  $10^7 \Omega$  [30,31] and Tseng and Ellenbogen estimate the resistance of Ellenbogen's resonant-tunneling transistor at  $10^7 \Omega$  [1]. With an operating between 1 and 5 V, these resistances lead to currents during a read operation of around 100 nA. From Equation (7), this current, combined with a bitline capacitance of  $2.6 \times 10^{-16} \text{ F}$ , produces a voltage change  $\Delta V$  of 0.025 V in approximately 0.1 nanoseconds<sup>1</sup>. However, it is not known precisely how the resistance of a Tour wire changes as its length is increased. Electrons may be conducted through molecular wires by a variety of mechanisms, some of which may be length-independent and some of which may decrease linearly or even exponentially as molecular length increases [33]. If it is assumed that, overall, Tour wire resistance increases approximately linearly with length, as does the resistance of macroscopic wires, then the access time increases to 100 nanoseconds. If the resonant-tunneling transistor turns out to be more or less resistive than estimated, this will also affect the time of a read operation. Such concerns were ignored above in preceding RAM performance calculations. This is because the memory was found not to be functional due to capacitance problems or it was assumed that the most resistive and speed-limiting component in the memory would be the NDR devices. This issue will be discussed in greater detail below.

## **EXTRAPOLATION OF MICROELECTRONIC MEMORY PROPERTIES**

This section considers the scaling of microelectronic memory down to the size of molecular memory circuits under the assumption that classical laws of electronics do not break down at the nanometer scale as a result of quantum mechanics or other small-scale effects. The results of this "extrapolated" microelectronic memory, along with the properties of conventional memory, are shown in Table 3 on the following page.

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<sup>1</sup> The capacitance is twice that of a bitline in NDR-based because the 4-Transistor SRAM will be approximately twice as long and wide as the NDR-based RAM cell [10]

**Table 3. Classical extrapolation of micron-scale RAM properties to the molecular scale**

	Cell Size (nm <sup>2</sup> )	Wire Width & Height (nm)	Wire Length (μm)	Max BL Cap. (F)	Bitline Resist. (Ω)	Transistor Resist. (Ω)	NDR Device Resist. (Ω)
<b>Micron Scale</b>							
<b>DRAM</b>	0.26x10 <sup>6</sup> [12]		890	1.0x10 <sup>-13</sup>	77		
<b>NDR-RAM</b>	1.2x10 <sup>6</sup> [10]	360, 504 [24]	1,500	1.2x10 <sup>-13</sup>	130	18,000 [12]	100,000 [25]
<b>SRAM</b>	4.6x10 <sup>6</sup> [34]		2,500	1.4x10 <sup>-13</sup>	220		
<b>Nm Scale</b>							
<b>DRAM</b>	30		9.6	1.0x10 <sup>-15</sup>	7,000		
<b>NDR-RAM</b>	140	3.9, 5.5	16.1	1.1x10 <sup>-15</sup>	12,000	1.7x10 <sup>6</sup>	9.3x10 <sup>6</sup>
<b>SRAM</b>	530		27.6	1.3x10 <sup>-15</sup>	20,000		

The cell sizes, wire widths and heights, and device resistances for conventional memory were taken from several sources [34]. Values are used from the 180-nm “technology node” – an indicator of the minimum scale of circuit components in a generation of electronics – from the ITRS [12]. To extrapolate these properties down to the molecular scale, this investigation considers memory at a hypothetical 1.9-nm technology node, which approximately corresponds to the cell size of ME-TSRAM. Wire lengths, widths, and heights, cell widths and heights, transistor dimensions and the spacing between devices are assumed to decrease linearly with the technology node. The thickness of the substrate on which the memory is built is held constant at 2.5 microns, the minimum DRAM layer thickness from the ITRS [12]. The cell capacitance also is held constant at 25 fF, because according to the ITRS, this is the minimum capacitance with which a DRAM cell can function.

Bitline capacitance is calculated using an approach described by R. Ho *et al* [24]: modeling the wire as four parallel-plate capacitors – two for capacitance with adjacent wires and two for capacitances to wires or plates above or below the wire – plus a term for the fringe capacitance. This approach yields the equation:

$$C = 2\epsilon_{horiz}L\frac{thick}{spacing} + \epsilon_{vert}L\frac{width}{ILD_{thick}} + \epsilon_{sub}L\frac{width}{SUB_{thick}} + C_{fringe}, \quad (10)$$

in which *thick*, *width*, and *L* are the thickness (height), width, and length of the wire. The parameters  $\epsilon_{horiz}$ , and  $\epsilon_{vert}$ , and  $\epsilon_{sub}$  represent the dielectric permittivities of the material between adjacent bitlines, between wiring levels, and of the substrate, while  $ILD_{thick}$  and  $SUB_{thick}$  are the thicknesses of the dielectric between

wiring levels and of the substrate. For conventional silicon technology,  $\epsilon_{horiz} = 3.72\epsilon_0$ ,  $\epsilon_{vert} = 4.1\epsilon_0$ , and  $\epsilon_{sub} = 4.1\epsilon_0$ , where  $\epsilon_0$  is the permittivity of free space [24]. The first term is for the worst-case maximum capacitance between a bitline and the adjacent bitlines to the left and right.<sup>2</sup> The second two terms, respectively, describe the capacitances between the wire and the above wiring level and between the wire and the ground plane. It is assumed that the separation between wiring levels is equal to the height of the wires. The fourth term is the fringe capacitance, which makes up approximately 9.3% of the worst-case wire capacitance in normal circuits [24]. The worst-case capacitance in memory arrays is not as high and thus fringe capacitance makes up 13.7% of bitline capacitance. It is assumed that this percentage holds constant as memory is miniaturized, although this will give an underestimate because fringe effects are expected to play a larger role in wire capacitance as wires get smaller.

The resistance of the bitline can be determined with the formula:

$$R = \rho L/A, \quad (11)$$

where  $L$  and  $A$  are the length and cross-sectional area of the bitline and  $\rho$  is the resistivity of the bitline material ( $1.56 \times 10^{-8} \Omega\text{-m}$  for copper) [18]. The device resistance should be inversely proportional to the technology node, and thus increases as the memory is scaled down.

The access times in Table 1 for the dynamic and static RAM on are from Equations (6) and (7), respectively, and the properties listed in Table 3.

## DISCUSSION

A comparison of the classically extrapolated nanometer-scale memory properties and the calculated molecular-scale memory properties suggests that scaling charge-storing memory down to the molecular scale will increase the memory's resistance and decrease its capacitance beyond the classical effects of scaling.

The molecular bitline capacitance was calculated to be approximately one order of magnitude less than the extrapolated solid-state bitline capacitance. This is the result that one would expect intuitively –

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<sup>2</sup> The capacitance between adjacent wires is negligible when they are charged simultaneously. The worst-case

i.e., that the molecular capacitance would be lower than just classical laws would suggest. The addition of charge to a molecular capacitor is a larger percentage-wise change in molecules than in bulk copper wires.<sup>3</sup> In addition, the quantization of energy levels that occurs on the nanometer scale should make it more difficult to add charge to structures. However, the effects of these changes seem to be relatively insignificant, as the calculated molecular bitline capacitance is not much smaller than the extrapolated bitline capacitance.

The molecular storage node capacitances were much smaller than the extrapolated values. It was assumed that the cell capacitance in solid-state DRAM is constant because the ITRS insists that DRAM only can function with a storage node capacitance of at least 25 fF [12]. The capacitances of nanometer-scale structures that have been considered as storage nodes have all been approximately 0.01 aF [1], which is more than  $10^6$  times smaller. Although this difference may partially be a function of the nanometer-scale storage nodes considered, it seems likely that below a certain cell size, it must become impossible to maintain a capacitance of 25 fF. A 25 fF capacitor must have 160,000 electrons stored on it to be charged to 1 volt. As the memory cell is scaled down, it eventually must reach a point where a potential of 1 volt cannot possibly hold this many electrons in so small a volume. Further research is needed to better quantify such limits on nanometer-scale capacitance. Fortunately, the reasons for the minimum storage node capacitance in the ITRS – long enough data retention times and soft error immunity – do not necessarily apply to molecular-scale memory. The latch in an NDR-based memory cell prevents leakage currents from causing the slow loss of the stored bit. Thus, retention times are probably not an issue. The high-energy cosmic radiation or alpha particles that cause soft errors in RAM [26] would probably destroy the components of nanometer-scale memory. Molecular computers will need to be built using error-tolerant and fault-tolerant architectures instead of trying to maintain a high enough capacitance within memory cells to prevent soft errors. Such architectures already are being considered for other reasons – e.g. because the

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capacitance occurs when a bitline is activated but the neighboring bitlines are not.

<sup>3</sup> Given the density and atomic mass of copper and the fact that each copper atom gives one conduction electron, the bitline in the conventional DRAM listed in table 1 or 3 should have around  $1.4 \times 10^{16}$  free electrons. Charging the wire up to 1 volt corresponds to adding 690,000 electrons, which is an increase of 0.00000005%. Charging up to 1 volt a

chemical processes used to fabricate molecular computers will not have perfect yields and thus some percentage of molecular computer devices will be non-operational. This is discussed in further detail elsewhere [2,27].

It is more difficult to draw a meaningful conclusion from a comparison of the extrapolated and calculated resistances because of the uncertainty in the resistances of molecular-scale devices. At first glance, resistance values seem to radically increase. A five-nanometer-long Tour wire has a resistance of  $10^7 \Omega$ , three orders of magnitude larger than the extrapolated resistance of an entire copper bitline, and 30 G $\Omega$  resistance of the molecular NDR device is about four orders of magnitude greater than the extrapolated NDR resistance. Molecular NDR devices that operate through quantum tunneling have had measured resistances as high as  $10^{14} \Omega$ . However, these numbers can be misleading. It is thought that much of the resistance in these measurements came from the contacts to which the molecules were connected, rather than from the molecules themselves [28,29]. Thus, these molecular devices may exhibit much lower resistances when bonded to other molecular devices in a circuit, which could make the performance of molecular-scale memory better than the predictions of this investigation. In addition, it is not known precisely how the resistance of a nanometer-scale wire changes with its length. Resistance could increase linearly with length or not be dependent on length at all, or it could increase exponentially with length. However, the fact that essentially the same resistance was experimentally measured for a single benzene ring [30] and a three-ring polyphenylene wire [30,31] suggests that contact resistance dominated in these experiments or some mechanism of conduction through such structures is length-independent.

## SUMMARY AND CONCLUSIONS

The preceding analysis has shown that some nanometer-scale memory designs probably cannot be made to function using existing molecular devices. Nonetheless, it should be possible to build molecular-scale memory that operates nearly as fast as present-day memory and stores information 20,000 times more densely. The analysis also has shown that quantum effects are likely to decrease the capacitance and

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molecular bitline that has around 120,000 free electrons corresponds to adding about 110 electrons, which is an increase of 0.091%.

increase the resistance of molecular-scale circuit components. However, these effects should be small enough that they will not prevent the operation of charge-storing memory on the nanometer-scale.

This is an especially important insight because a number of proposals for molecular-scale memory use mechanisms other than storing charge to store a bit. In particular, there have been a number of proposals to use electromechanically induced conformation changes in molecules [15,17,35]. From the present work though, it appears that four decades of industrial experience with stored-charge random access memory arrays need not be discarded as we shrink memory down to the molecular scale. Charge-storing memory still has the potential for application at very much larger densities than in the present day, and, perhaps, for entirely new and as yet unimagined application areas.

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