Clocking Nanocircuits for Nanocomputers and Other Nanoelectronic Systems

Shamik Das and Matthew F. Bauwens
Nanosystems Group
The MITRE Corporation
7515 Colshire Dr., McLean, VA 22102, USA
{sdas,mbauwens}@mitre.org

***Abstract*— Prospective performance bounds are determined by simulation for a class of all-nanoelectronic clocking circuits. Such nanocircuits could be utilized as on-chip master clocks for stand-alone nanosystems, as local clocks within nanoelectronic computers, or as local oscillators in mixed-signal nanoelectronic applications. Designs and simulation results are presented for these nanocircuits, which are intended to be manufacturable using presently available nanodevices and nanofabrication techniques. The results presented here indicate that such clocking nanocircuits, if built using presently available devices, could achieve operating frequencies up to approximately 1 GHz for analog applications and 150 MHz for digital nanoelectronic systems.**

I. Introduction

There has been much progress over the past several years in the design and development of nanocomputer systems integrated on the molecular scale [1–35]. In particular, functioning prototypes for extended nanoelectronic memory systems [30, 34] recently have been demonstrated. These recent results suggest that the fabrication of complex nanoprocessing systems should be possible in the near future.

Two general approaches are being pursued for the development of such systems. The first approach, "hybrid" CMOS/nano systems, involves the integration of nanoelectronic devices with conventional silicon CMOS technology [25,27,35]. The second approach has the goal of designing and fabricating nanocomputer systems composed entirely of post-CMOS nanoelectronic devices. Over the long run, this second approach may lead to capabilities that will be more transformative, especially when considering a range of applications from high-performance, general-purpose nanocomputing systems to embedded, special-purpose nanoelectronic circuits. Thus, it is upon such all-nanoelectronic nanosystems that we focus here.

To address the challenges inherent in the design of these nanoelectronic systems, researchers have had to invent entirely new system architectures. Because of the great complexity of devising such architectures, architects have focused almost entirely on the most pressing challenge, that of designing the functional or logical components of nanocomputers, i.e., the datapath [3]. These efforts have resulted in a variety of approaches [18, 21, 22, 24, 31] that incorporate detailed considerations of logic synthesis for nanoelectronic systems.

However, nanocircuits beyond the datapath are required to implement a complete nanocomputer. In particular, control structures and signals also are needed. One control structure that must satisfy stringent performance constraints is the clock generation and distribution structure for a nanoelectronic system. Analysis of an all-nanoelectronic clock circuit would provide insight into the challenges and the prospective performance of a nanoelectronic computer system.

nanodevice	clock frequency	V_{DD}	# stages	ref.
multiple CNTs	5 Hz	1.5 V	3	[5]
multiple CNTs	220 Hz	4 V	3	[36]
nanowire transistors	11.7 MHz	43 V	3	[37]
single CNT	52 MHz	0.92 V	5	[38]

TABLE I. Experimentally demonstrated clock circuits using nanoelectronic devices. These circuits consist of ring oscillators built from nanoscale transistors and conventional lithographic-scale interconnects.

In Section II of this paper, designs and simulation results are detailed for a set of all-nanoelectronic clocking circuits. Section III discusses the integration and distribution of these clocking nanocircuits within a nanoelectronic system. Section IV concludes the paper.

II. Designs and Simulations for Clocking Nanocircuits

Table I lists recent experimental examples of clocking circuits built from novel nanoelectronic devices. As can be seen from the table, a wide range of clock frequencies and supply voltages has been demonstrated. For practical purposes, only the last two of these examples are fast enough for most digital logic applications.

However, the low oscillation frequency of the first two examples is not perceived to be an intrinsic limitation. Instead, the performance of the oscillators listed in Table I is limited primarily by the extensive use of micrometer-scale contacts and interconnects. Employed for expediency in fabrication and experimentation, these interconnects present a significant capacitive load to the very tiny devices that are used to constitute the oscillators. If these micrometer-scale wires were replaced with nanoelectronic wires, the performance of the oscillators should be much improved.

Thus, the designs presented in this paper are intended to be synthesizable using only nanoelectronic devices and interconnects. An example of an architecture for an all-nanoelectronic nanocomputer system is shown in Fig. 1. This architecture,

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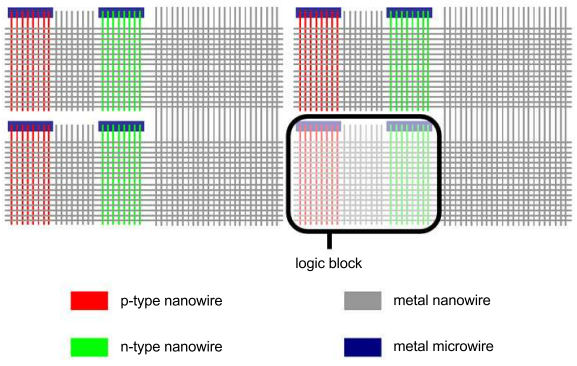

Fig. 1. Diagram of a nanowire-based system architecture for programmable logic, as proposed by Snider *et al.* [22]. In this architecture, semiconducting and metallic nanowires are patterned in crossed-wire arrays that can be utilized to implement reconfigurable logic circuits. The basic array unit, the logic block depicted here, can be tiled to form larger logic structures. The circuits implemented within the logic blocks are interconnected using the columns of long metallic nanowires depicted in the diagram.

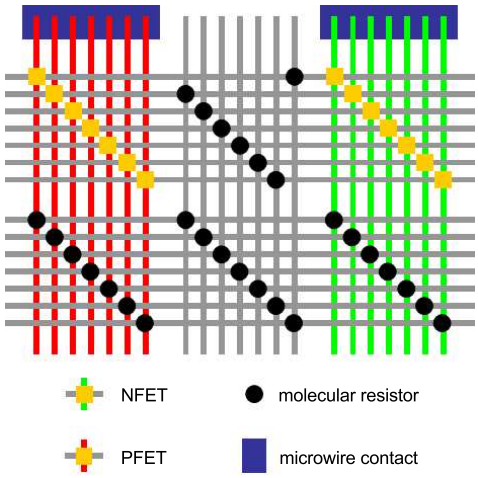

Fig. 2. Layout of an all-nanoelectronic clock circuit. This circuit is a seven-stage ring oscillator composed of nanowire transistors and programmable molecular resistors. It is laid out according to the architecture depicted in Fig. 1.

proposed by Snider *et al.* [22] and called the complementary/symmetry array, consists of an array of tiles of nanowire crossbars. These tiles or logic blocks consist of a small number of nanowire transistors that may be configured to produce small logic circuits. These circuits may be interconnected using the columns of long nanowires shown in the figure.

The complementary/symmetry architecture readily lends itself to implementation of feedback circuits such as ring oscillators. Five oscillator circuits are considered here, consisting of three to eleven stages. Fig. 2 depicts a layout diagram for the seven-stage ring oscillator. In this figure, horizontal metal nanowires are overlaid over clusters of vertical p-type (red), metal (gray), and n-type (green) nanowires. The metal-semiconductor junctions in the upper half of the circuit can be programmed individually such that selected junctions, denoted by yellow boxes in the figure, represent field-effect transistors [22, 39]. The remaining junctions are composed of programmable (hysteretic) molecular resistors [10, 40–42]. When extrapolated to a 10 nm by 10 nm crossed-nanowire junction, these resistors can be programmed to have resistances as low as 1-100 MΩ (denoted by black dots in the figure) or as high as several GΩ (all other junctions).

For these nanocircuit designs, simulations were carried out using the Cadence DFII software package [43]. The simulation methodology [3, 44] was as follows. First, empirical data were obtained for the desired nanodevices and interconnect structures, such as experimentally demonstrated p-type and n-type nanowire transistors [39]. Second, these data were encapsulated into Verilog-A models [3, 44]. Third, system-level schematics were assembled within the Cadence Virtuoso environment [43] to represent Fig. 2 and the designs for the other oscillators. Finally, the performance of the circuits was simulated using the Cadence Spectre simulator [43].

The results of these simulations are given in Figs. 3 and 4. Fig. 3 shows the range of achievable frequencies for the five ring oscillators simulated here. As can be seen in the figure, clock frequencies of up to 1 GHz are obtainable using presently available devices. The clock waveforms that can be generated may be grouped into two classes. The waveforms above approximately 150 MHz are generated by relatively high supply voltages (4 - 10 V) and tend to be sinusoidal. Thus, these waveforms are suited best for analog RF applications, such as VHF or UHF communications, rather than for digital nanosystems. Waveforms at 150 MHz and below can be generated using lower supply voltages. Also, since these slower oscillators use more stages, their outputs tend to be more square, with slew rates exceeding 8000 V/μs and rise/fall times of less than 1.6% of the clock period (measured at 3 V supply). Thus, these oscillators are more suitable for digital logic. Fig. 4 provides greater detail for this subset of oscillators.

Many present digital applications operate at speeds below 150 MHz and could take advantage of the much smaller chip areas made possible by nanoelectronics. Examples include some microcontrollers, digital signal processors, and custom integrated circuits. Nanoelectronic system designs have been developed previously for externally-clocked components of some of these applications [45]. The following section examines how a clock circuit might be integrated and distributed within such systems.

III. Clock Integration and Distribution in a Nanoelectronic System

In order to implement synchronous logic in the complementary/symmetry architecture, a global clock signal must be distributed to all of the logic tiles. The most straightforward way for this to be done is to drive the global clock onto the long nanowires (shown in Fig. 1) that span the tiles. In this approach, the clock skew is dictated by the interconnect delay

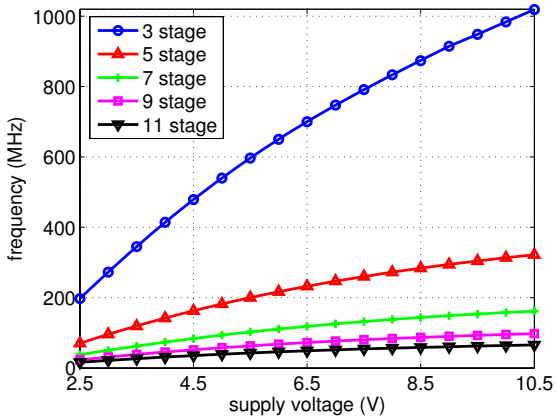

Fig. 3. Simulated frequency vs. supply voltage for various ring-oscillator nanocircuits.

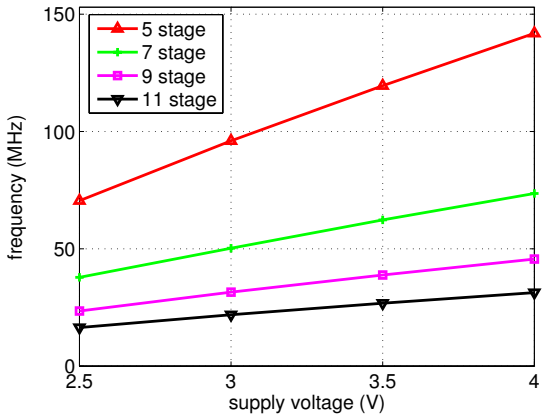

Fig. 4. Detail of the lower-left portion of Fig. 3. This graph identifies the frequencies achievable at reasonably low supply voltages and with enough stages to generate clock waveforms that are relatively square.

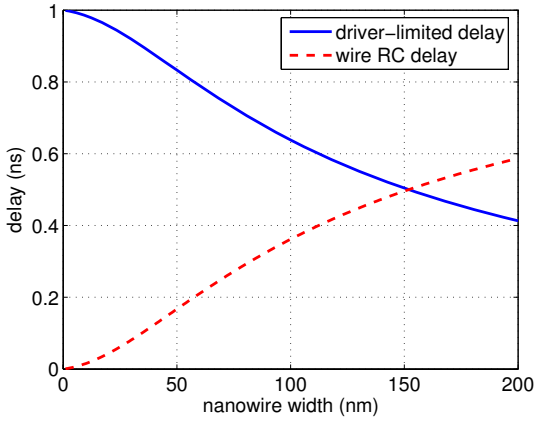

Fig. 5. Components of delay in a clock circuit consisting of a driver connected to a receiver. The driver and receiver are assumed to be composed of semiconducting nanowire transistors, and the interconnect is assumed to be a metal nanowire of the same width and height as that used for the transistors. For each given nanowire width, the length of the metal nanowire is selected so that the total delay is 1 ns.

from one end of the long nanowires to the other end. Thus, a maximum bound on clock skew will determine the maximum size of an array of contiguous tiles for this architecture. If larger arrays are desired, they must be constructed by tiling these maximal arrays and interconnecting them using repeaters or registers.

Specifically, for a square array of tiles such as is shown in Fig. 1, the clock signal must be transmitted along one vertical nanowire in each column. If, for example, the system clock is 100 MHz and 10% skew is to be tolerated in the clock edge, then the maximum delay in transmitting the clock signal to the end of the nanowire is 1 ns.

Given a few assumptions about the nanowires to be used, a calculation may be carried out to determine the maximum length of these nanowires. The assumptions are as follows.

- A single clock driver is connected to a single receiver via a nanowire.
- Both the driver and receiver are composed of silicon nanowire transistors [46]. The gate dielectric is silicon dioxide.
- The interconnect is a copper nanowire of the same width and height as that used for the transistors.
- The signal swing is assumed to be 1 V.

The length of the copper nanowire is chosen such that the total delay is 1 ns from the clock driver to the receiver through this wire.

There are two sources of this 1 ns delay. First, there is the delay arising from the clock driver impedance, plus the wire and receiver capacitances. Second, there is the RC delay due to the wire itself. Fig. 5 shows that at narrow nanowire dimensions, the driver impedance dominates the delay. This is because the drive current of the nanowire transistors must fall off as the nanowire width decreases, even if it is assumed that the typical MOSFET drive strength of approximately 1000 μA/μm at 1 V will be achievable in much narrower transistors [46].

At the narrow nanowire widths that are proposed for use in some all-nanoelectronic nanocomputers [18, 22, 31], the reduced current drive of the nanotransistors limits the length of nanowire that can be driven. This directly impacts the number of logic gates that can be driven by a clock signal. Fig. 6 shows how the number of gates per clock repeater scales with the nanowire width. For larger nanowires that approach lithographic wires in size, up to a hundred thousand logic gates can be driven by a given clock signal. However, for nanowires 20 nm or narrower, at most ten thousand gates can be supported. Furthermore, this analysis assumes the optimal usage of defect-free nanowire arrays. If there are fabrication defects, or if the desired logic networks cannot be designed to

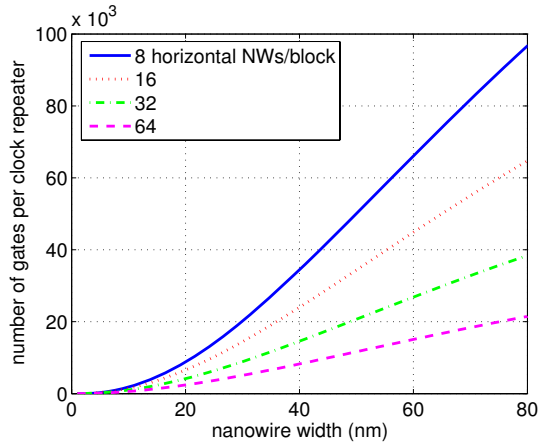

Fig. 6. Number of gates per 100 MHz clock repeater in the complementary/symmetry array. This figure depicts four different configurations of the logic blocks shown in Fig. 1. For each configuration, the number of horizontal nanowires per logic block is specified.

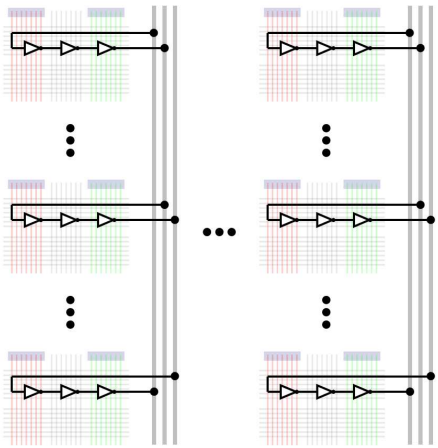

Fig. 7. Architecture for a distributed clock generator within a complementary/symmetry array. Here, a nine-stage ring oscillator is formed by distributing three-stage blocks across the tiles of the system. Three long nanowires from the routing column are used to distribute the three major phases of the clock. Each block may be repeated multiple times along the length of these long nanowires. This allows both the clock frequency and the skew to be controlled as the length of the routing column grows.

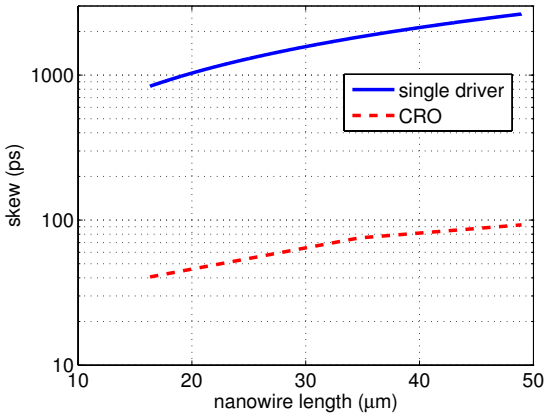

Fig. 8. Comparison of clock skew in two scenarios. The first scenario is the same as in Figs. 5 and 6: a single driver outputs the clock onto a long nanowire. In the second scenario, multiple cooperative ring oscillators (CRO) are distributed along the length of the nanowire, as shown in Fig. 7.

fit compactly within the available hardware, then the effective hardware utilization would be less than stated here.

Since the equivalent of 10^6 to 10^7 gates would be required to construct a complete, general-purpose nanoprocessor, such a system would need to be partitioned carefully into tens or hundreds of tile arrays. Alternatively, massively multicore or tile-based architectures such as Raw [47,48] might be considered. Or instead, novel clock distribution architectures from microelectronic processors might be adopted. One example is the globally asynchronous, locally synchronous (GALS) model [49, 50]. Using this model, each array of tiles in a nanoprocessor could have its own local nanoelectronic oscillator, with additional circuitry employed to communicate between tiles.

A similar approach to GALS that would require less communication overhead is the use of cooperative ring oscillators (CRO), which was proposed previously for microelectronic systems [51]. In this approach, multiple ring oscillators are used in parallel to generate a single global clock. The ring oscillators are distributed spatially across the entire system.

Fig. 7 shows how this might be done within the complementary/symmetry architecture. Within a column of this architecture, the phases of the global clock could be conveyed along the long column nanowires. A subset of the column's tiles could be utilized to implement inverters that connect the clock phases. The number of tiles is chosen to be proportional to the length of the column nanowires. For example, out of a set of 90 contiguous tiles, 30 could be used to implement ring oscillator stages, so that 10 three-stage ring oscillators are working in parallel. (In Fig. 7, the stages themselves contain three inverters, so that the ring oscillators consist of nine inverters.)

In this way, the number of clock drivers is proportional to the capacitive load. This allows the skew to grow linearly with nanowire length, as opposed to quadratically. Fig. 8 shows how the skew is improved using this method. A factor of 25 improvement is obtained for nanowires 10 nm wide and up to 50 μm long (equivalent to approximately 75 tiles).

These results demonstrate that circuit techniques can be used to alleviate potential nanodevice drawbacks such as low nanotransistor drive current and high nanowire resistance. More generally, the simulations presented here indicate that with presently available nanodevices, moderately complex synchronous digital circuits could be implemented as all-nanoelectronic systems. Simple controllers, DSPs, coprocessors, and other special-purpose digital logic systems are among the many examples.

IV. Summary and Conclusions

In this paper, designs for clocking nanocircuits have been evaluated for potential use in all-nanoelectronic systems. Five ring oscillator nanocircuits were considered. Based on simulations of these nanocircuits, all-nanoelectronic systems with operating frequencies of up to 1 GHz should be feasible, if built using presently available devices. This would enable a wide variety of digital and analog system applications. However, for digital systems, practical considerations limit the range of useful oscillator frequencies to about 150 MHz.

Such clock speeds, while not fast enough for true high-performance processing, nevertheless would enable digital nanoelectronic systems of significant complexity. Thus, the distribution of clock signals within these systems must be considered carefully. Either novel system architectures or novel clock distribution schemes will be required. One such scheme, the use of distributed cooperative ring oscillators, was investigated here. Simulations show this scheme to be useful for managing the generation and distribution of relatively fast clocks within a nanoelectronic system. Thus, from a systems perspective, prospects are excellent for the development of reasonably fast, specialized, ultra-compact digital and analog nanoelectronics.

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